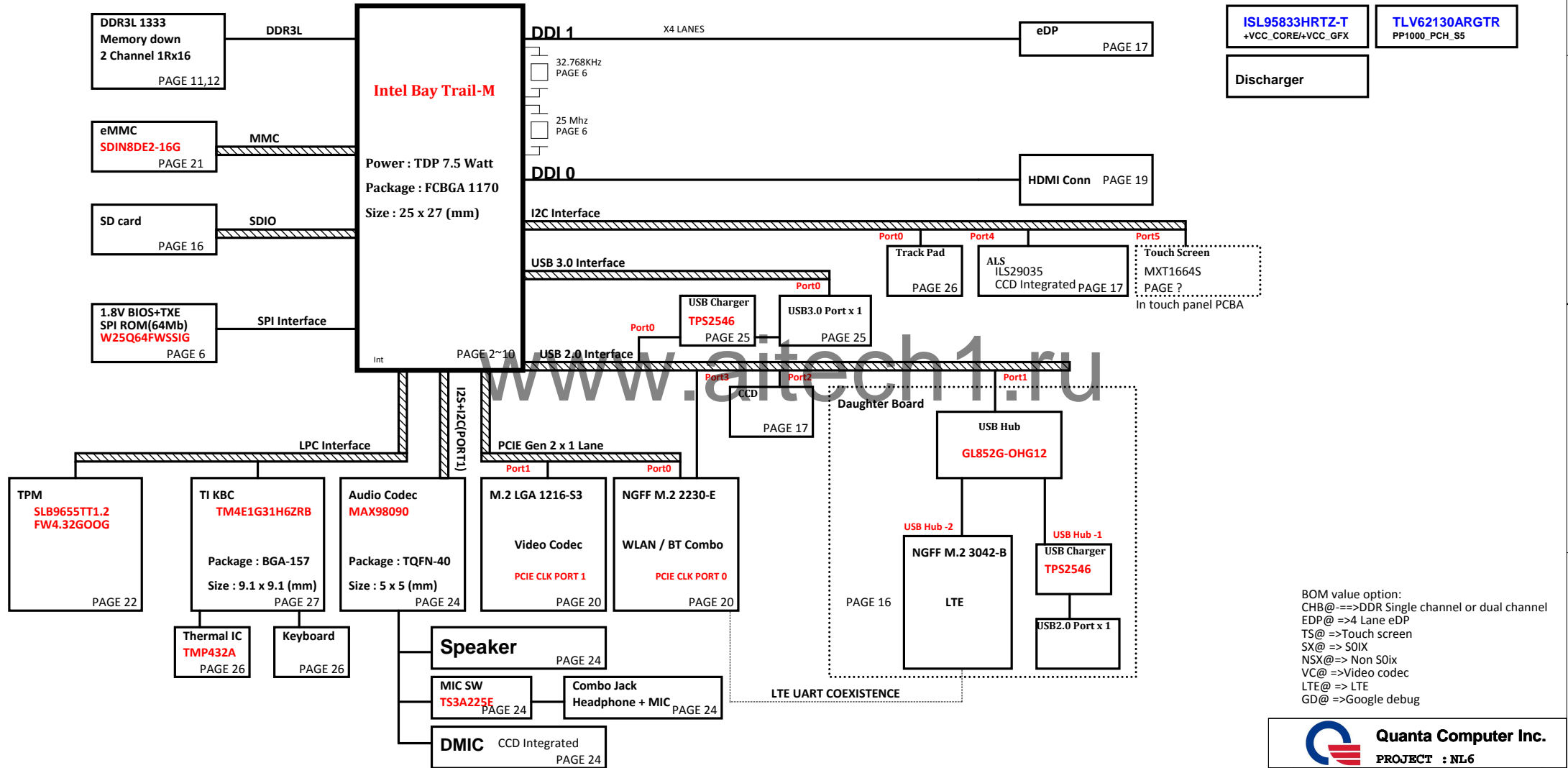


Intel Bay Trail-M Platform Block Diagram

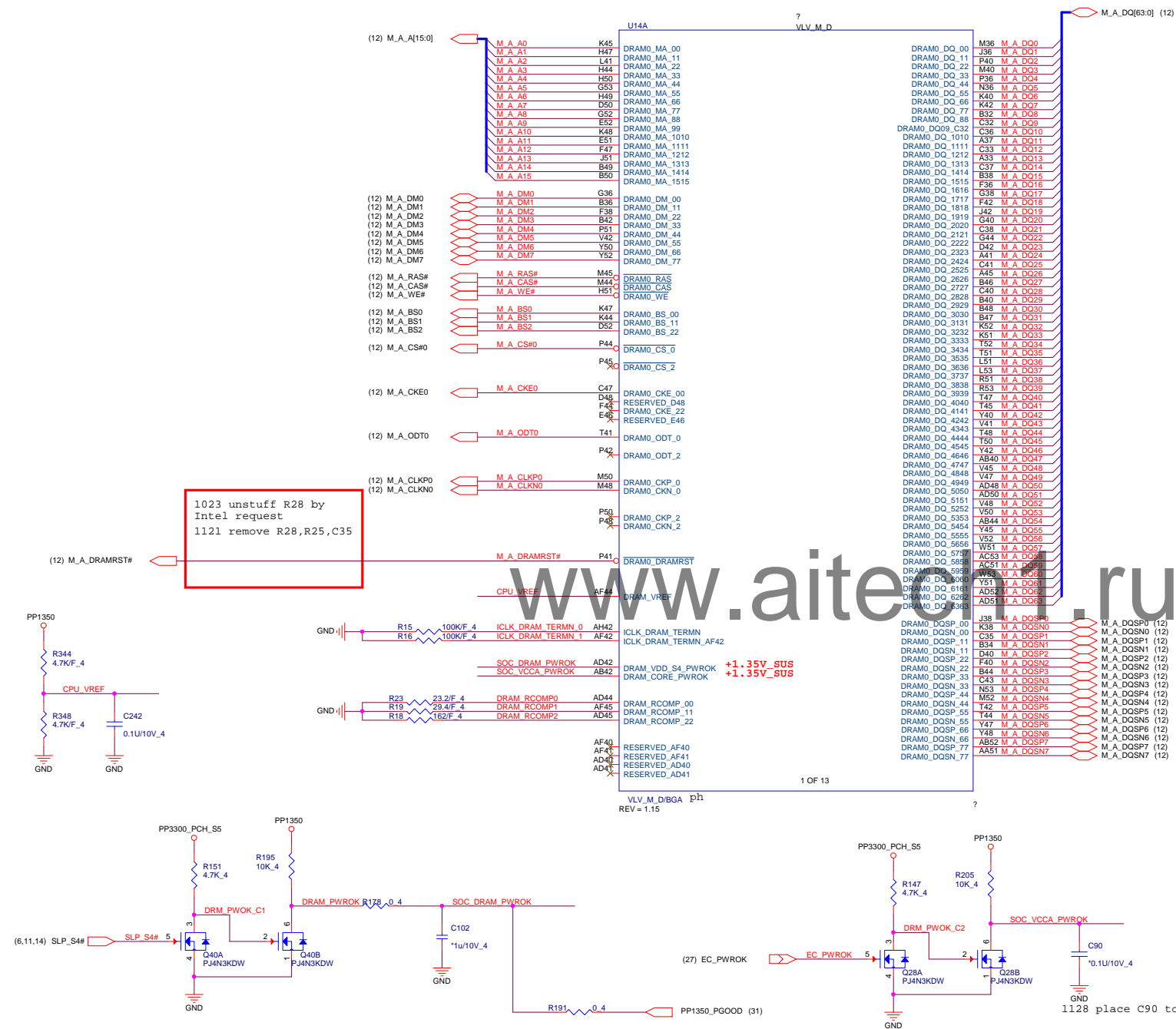
SKUA QC N2930
Up to 1.83 GHz SR1SG(FCBGA) P/N: AJ0QG9UUT01
SKUB DC N2830
Up to 2.17 GHz SR1SG(FCBGA) P/N: AJ0QG9VUT01

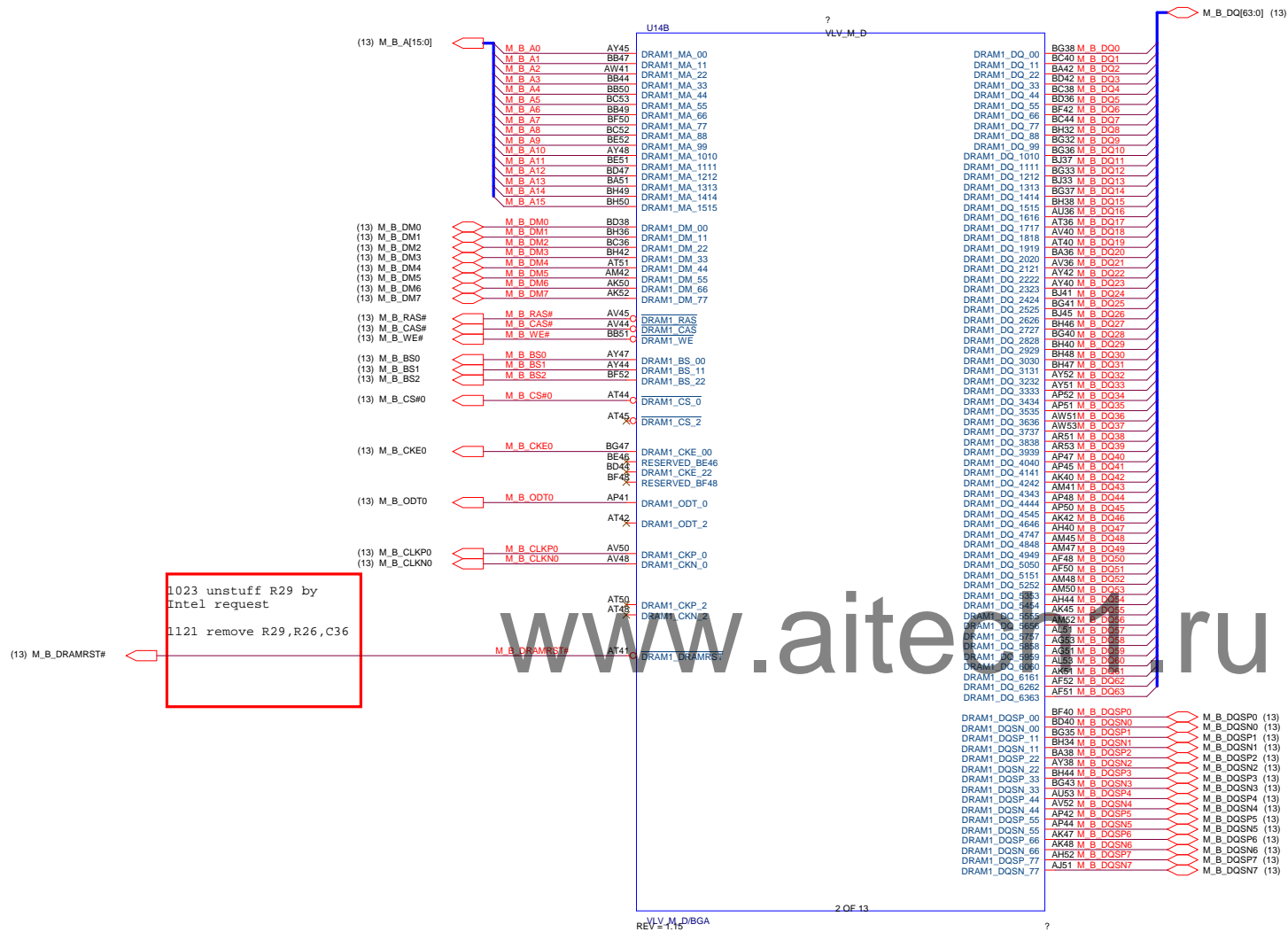


BOM value option:
CHB@ ==>DDR Single channel or dual channel
EDP@ ==>4 Lane eDP
TS@ ==>Touch screen
SX@ ==> S0IX
NSX@ ==> Non S0ix
VC@ ==>Video codec
LTE@ ==> LTE
GD@ ==>Google debug



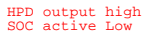
Quanta Computer Inc.
PROJECT : NL6





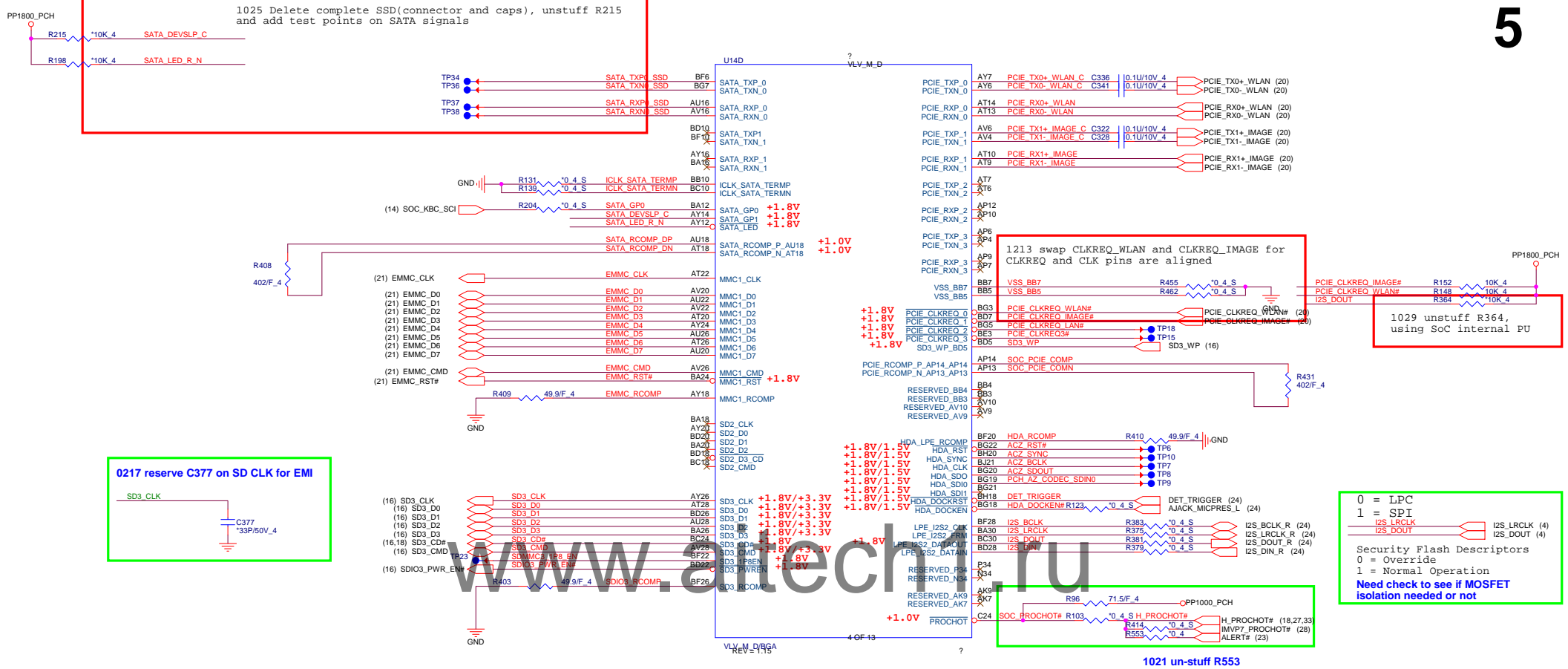
Quanta Computer Inc.
PROJECT : NL6

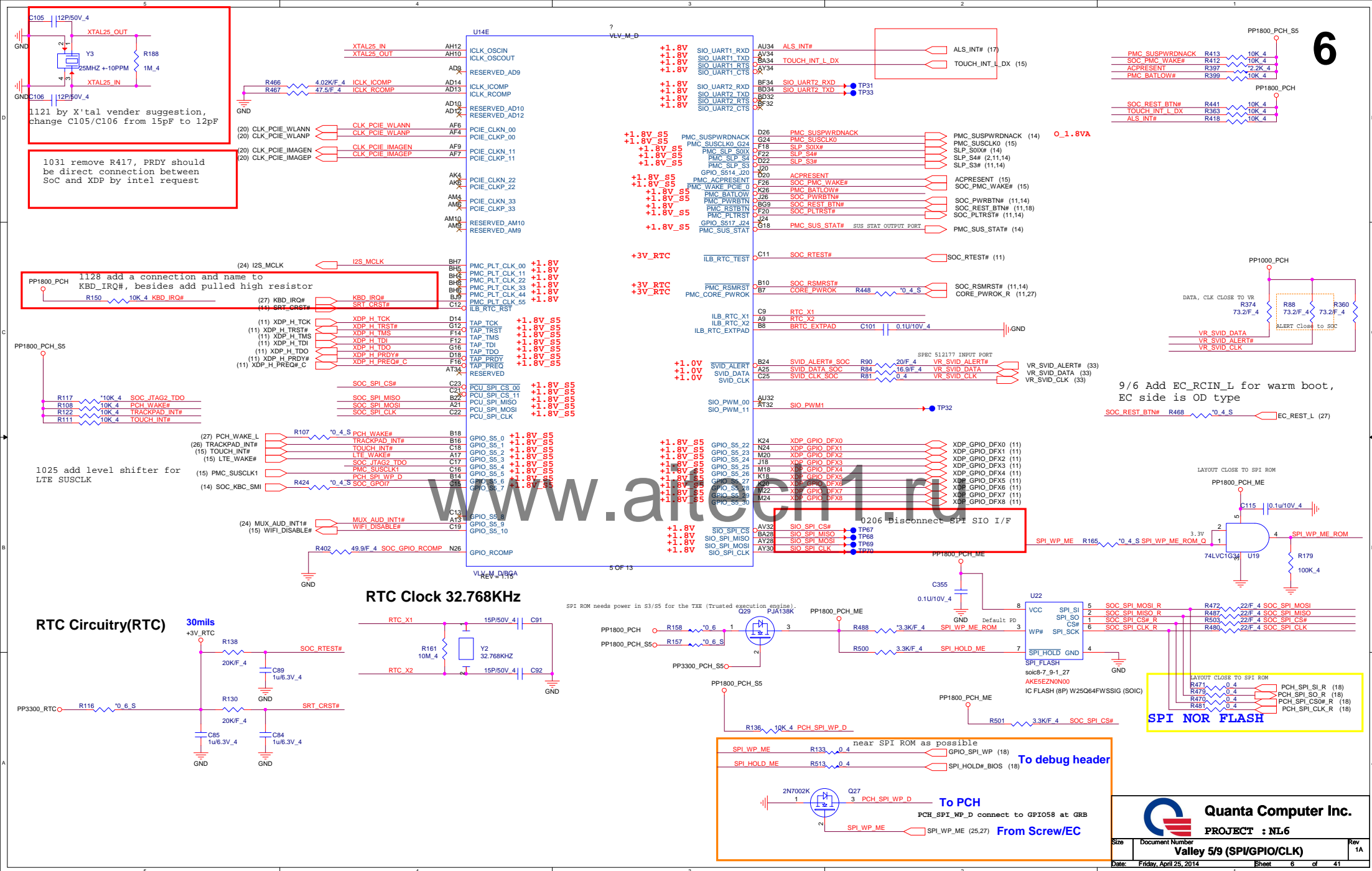
Size Document Number Valley 2/9 (DDR8) Rev 1A
Date: Friday, April 25, 2014 Sheet 3 of 41

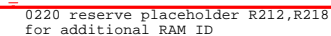


Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged 1 = Top address bit is inverted	(7) GPIO_SO_SC_56
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC 1 = SPI	(5) I2S_LRCLK
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override 1 = Normal operation	(5) I2S_DOUT
DDIO_DDCDATA	DDIO Detect	PWROK	0 = DDIO not detected 1 = DDIO detected	Pull up +1.8V at HDMI side
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDIO not detected 1 = DDIO detected	
GPIO_SO_NC_13				

```
1029 unstuff R386, using SoC internal PU
1115 stuff R386, it is required for eDP
```







Proto1/1.5 stage use H2G & H4G
1212 add new RAMID 101 for single channel SKU

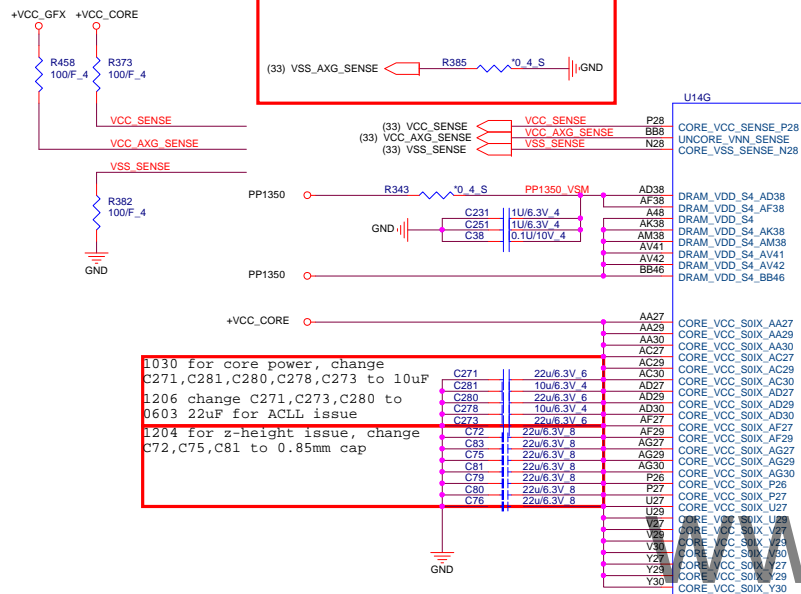


0220 R392,R389,R71,R65 need always to be stuffed even if w/o TS SKU



1031 for layout suggestion by intel, VSS_AXG_SENSE didn't connect to VSS_SENSE, will connect the GND via near VCC_AXG_SENSE
1031 for layout, add 0hm between GND and VSS_AXG_SENSE

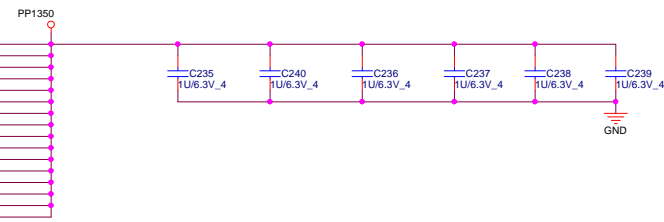
(33) VSS_AXG_SENSE \leftarrow R385 \rightarrow 0.4 S \rightarrow GND



1030 for core power, change C271, C281, C280, C278, C273 to 10uF
1206 change C271, C273, C280 to 0603 22uF for ACLL issue
1204 for z-height issue, change C72, C75, C81 to 0.85mm cap

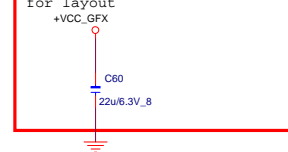
REV = 1.15 1031 remove TP44 and TP35 for GND vias adding

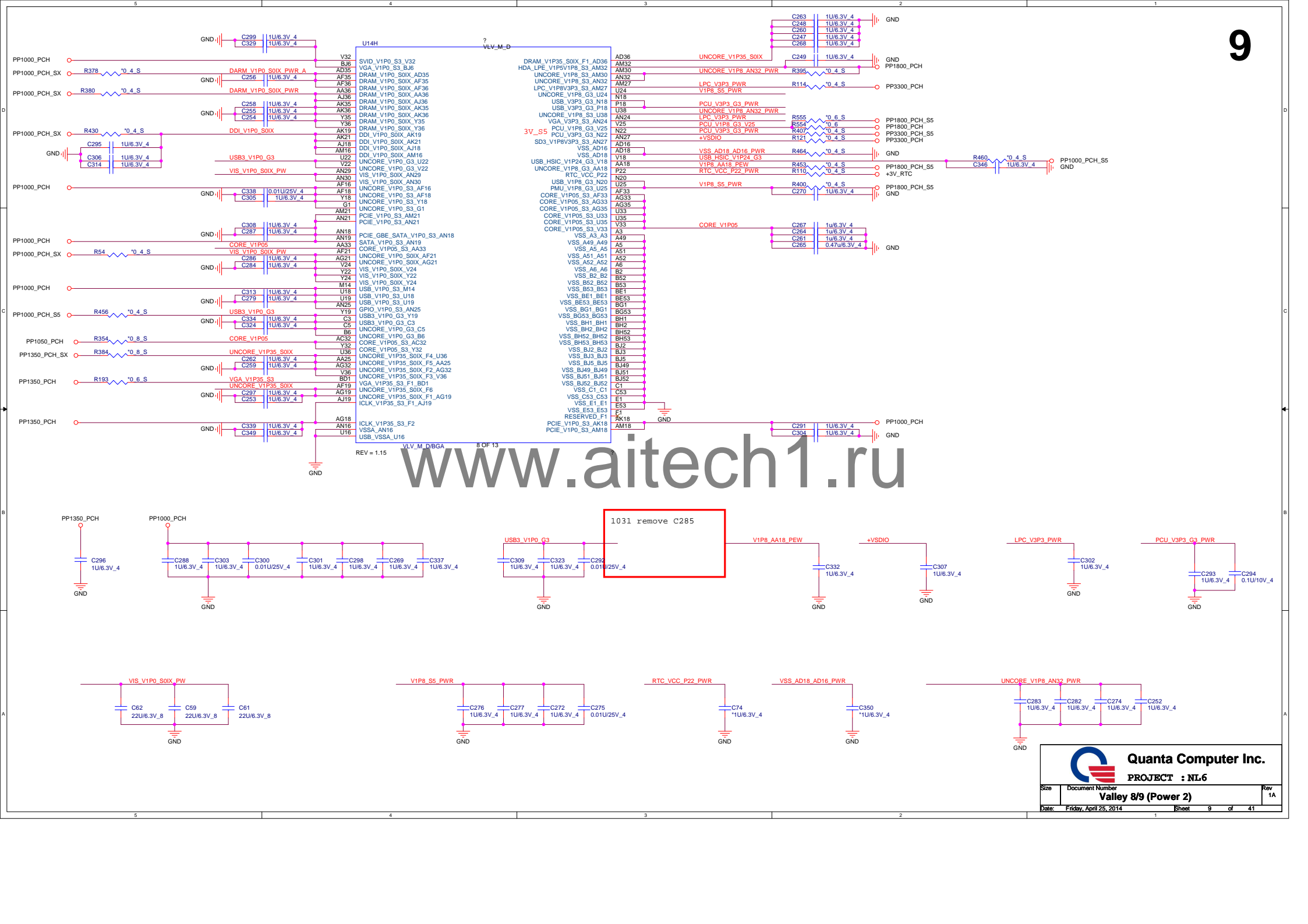
DRAM_VDD_S4_BD49
DRAM_VDD_S4_BD52
DRAM_VDD_S4_BD53
DRAM_VDD_S4_BF44
DRAM_VDD_S4_BG51
DRAM_VDD_S4_BJ48
DRAM_VDD_S4_C51
DRAM_VDD_S4_D44
DRAM_VDD_S4_F49
DRAM_VDD_S4_F52
DRAM_VDD_S4_F53
DRAM_VDD_S4_H46
DRAM_VDD_S4_M41
DRAM_VDD_S4_M42
DRAM_VDD_S4_V38
DRAM_VDD_S4_Y38

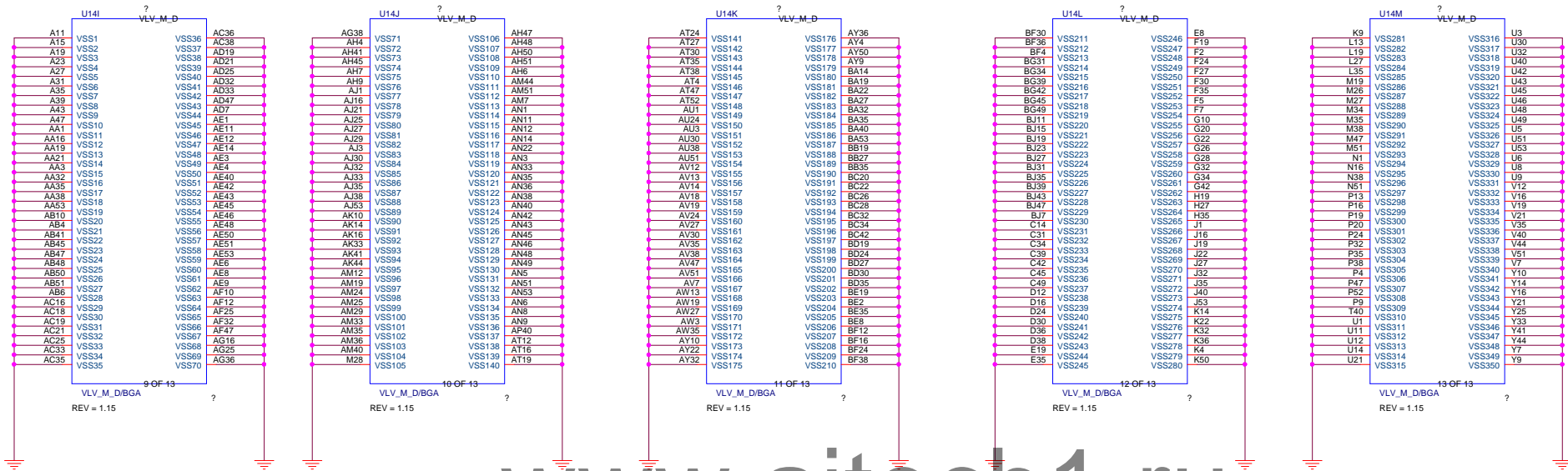


1030 for Gfx power, change C266, C289, C290 to 10uF and add 2 caps 10uF
1206 change C266, C311, C315 to 0603 22uF for ACLL issue

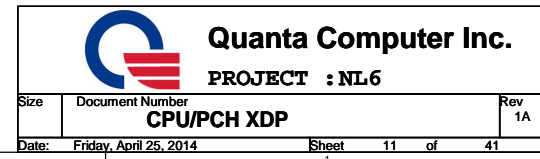
1030 change C60 power netname for layout

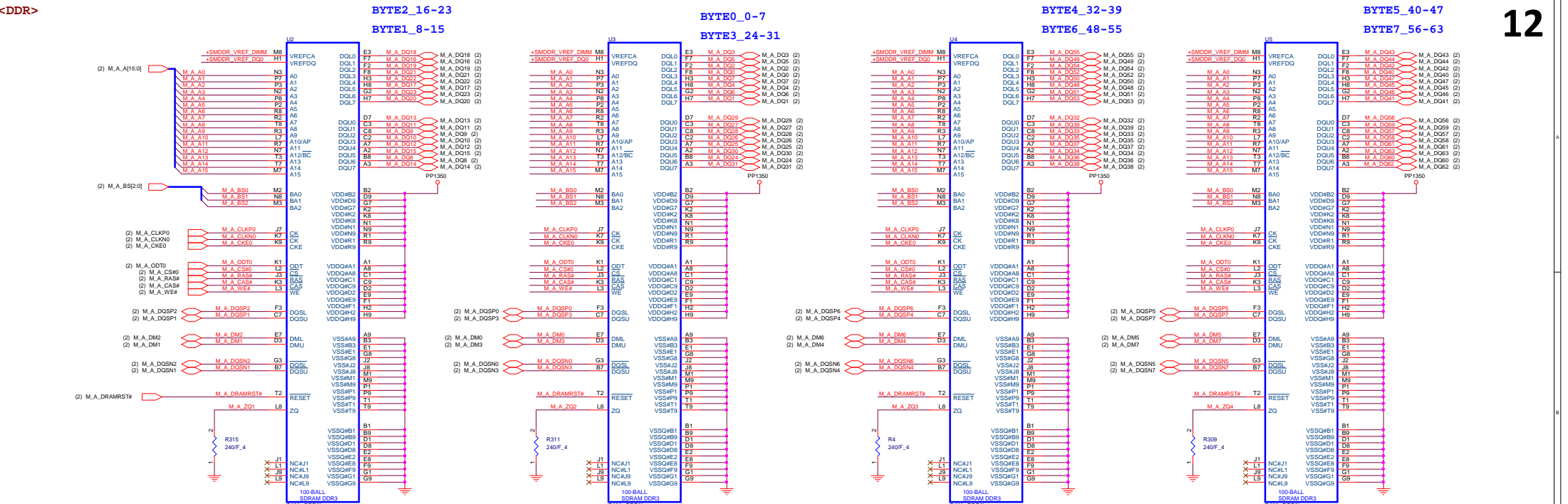




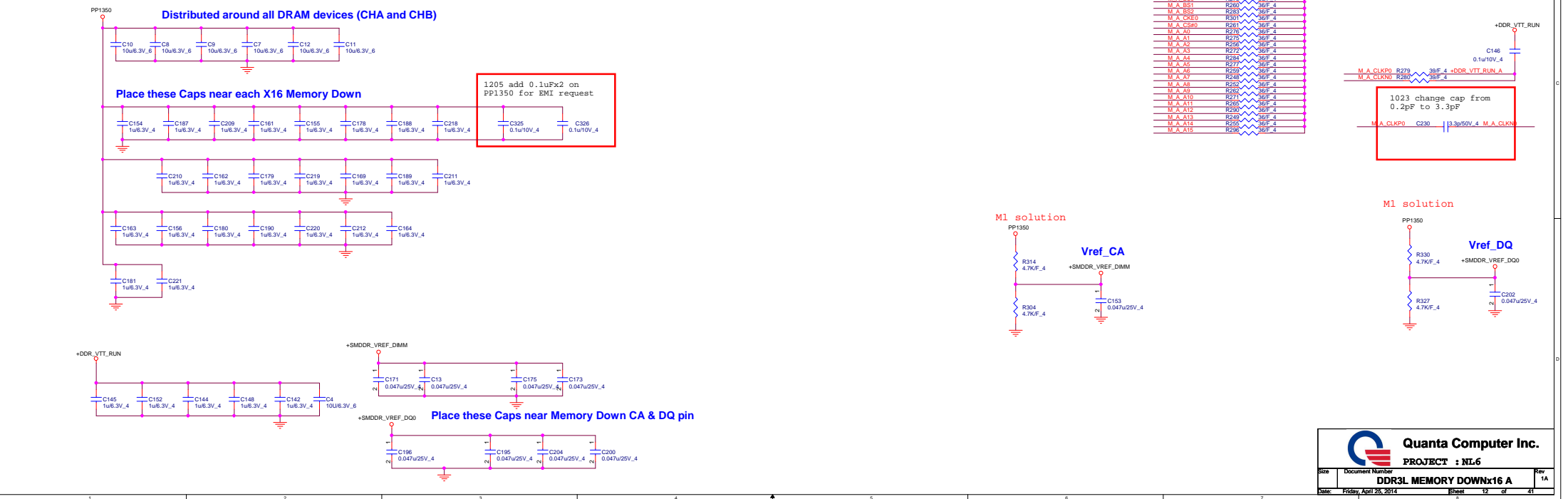


11



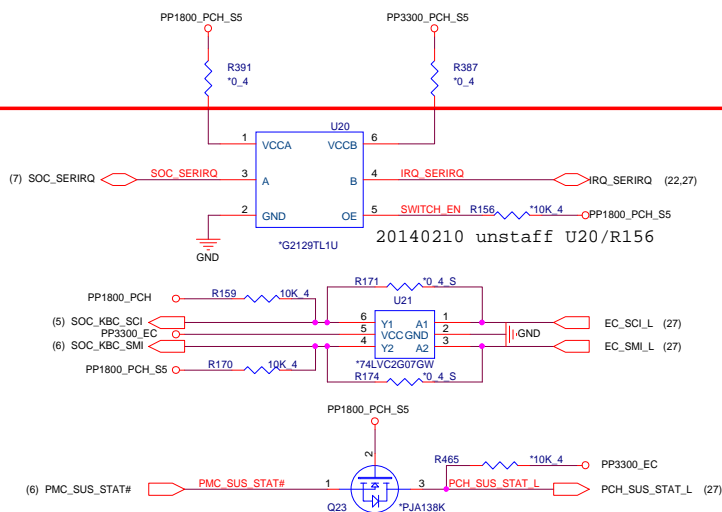


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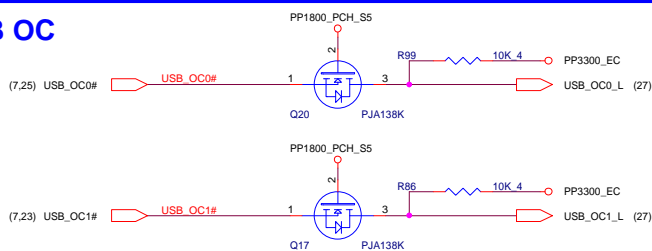


PWRON SEQUENCE

```
9/6 EC table says SERIRQ is OD pin, reserve for debugging
1128 remove R166, because SERIRQ of TPM needs 3V
1128 reserve 0 ohm R387/R391 on VCCA and VCCB for debugging
20140210 unstaff R387/R391
```

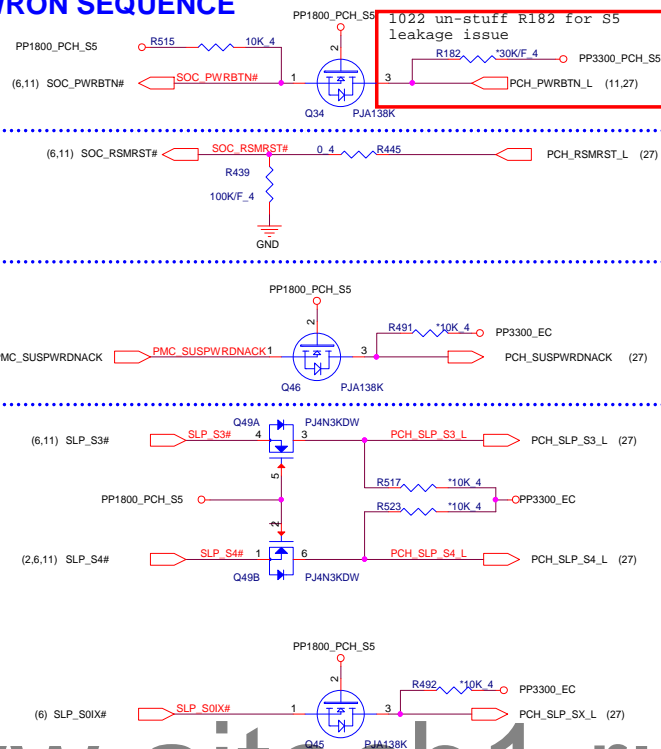


USB OC



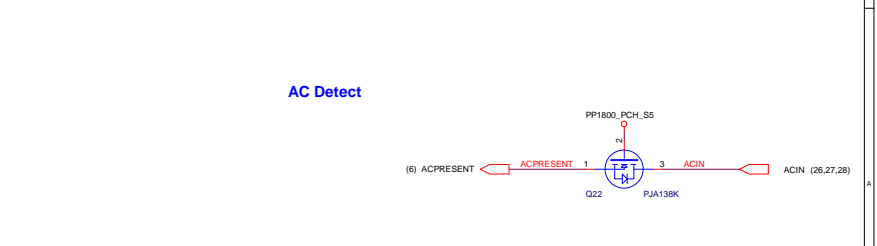
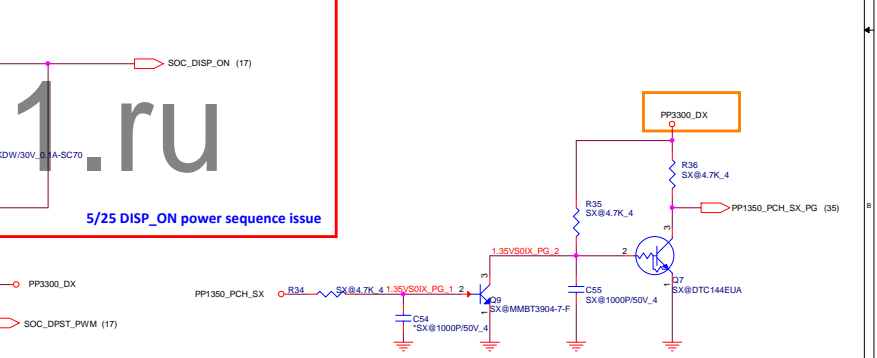
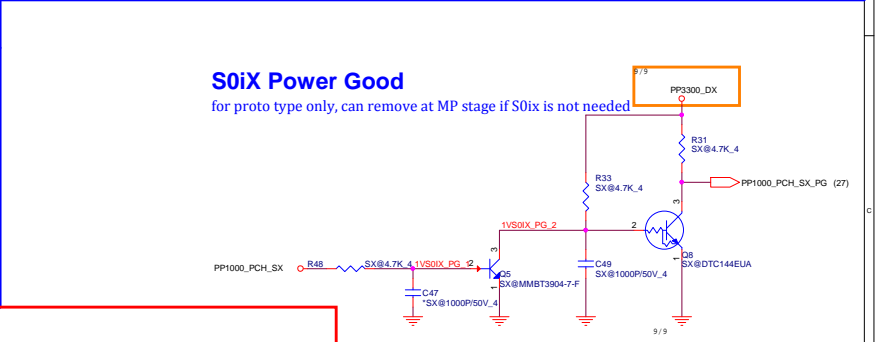
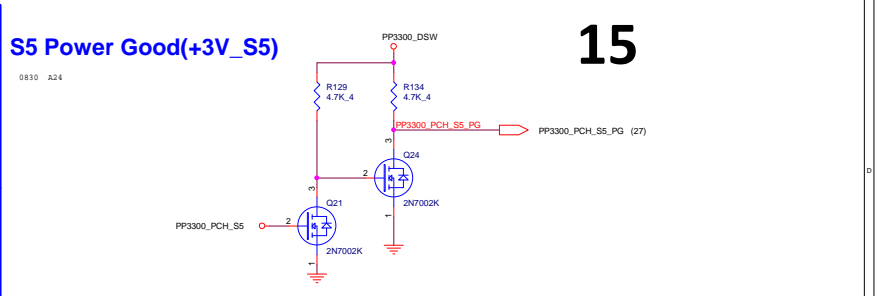
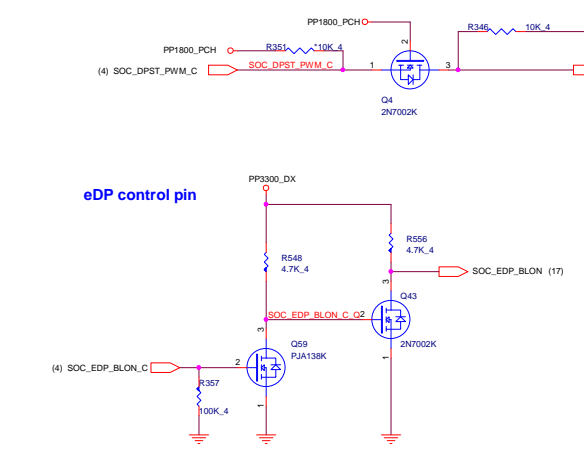
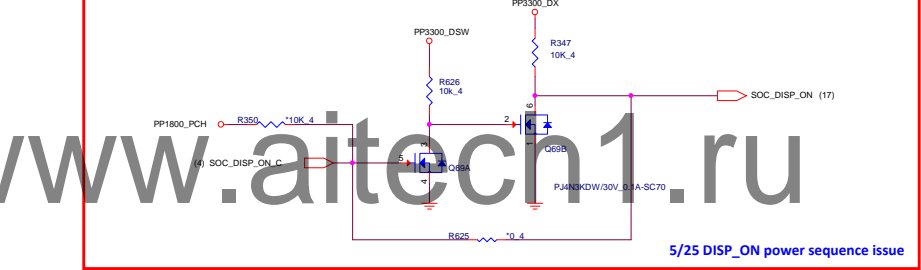
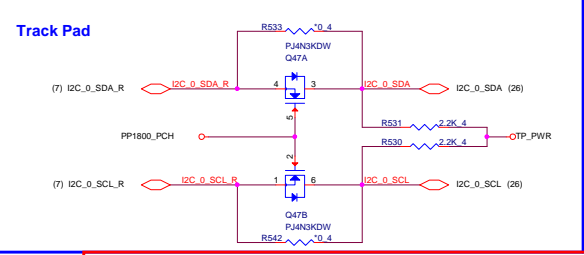
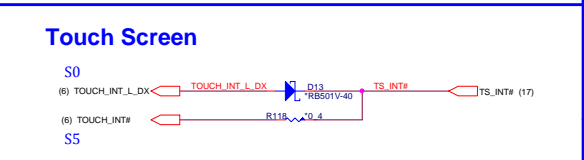
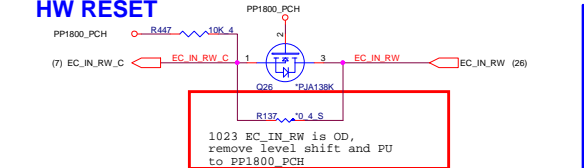
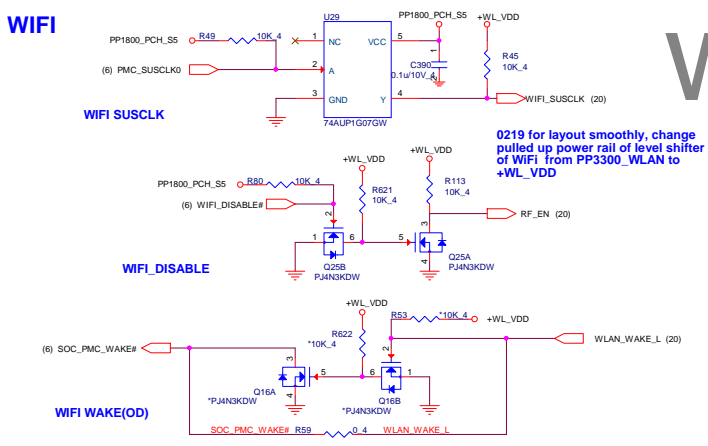
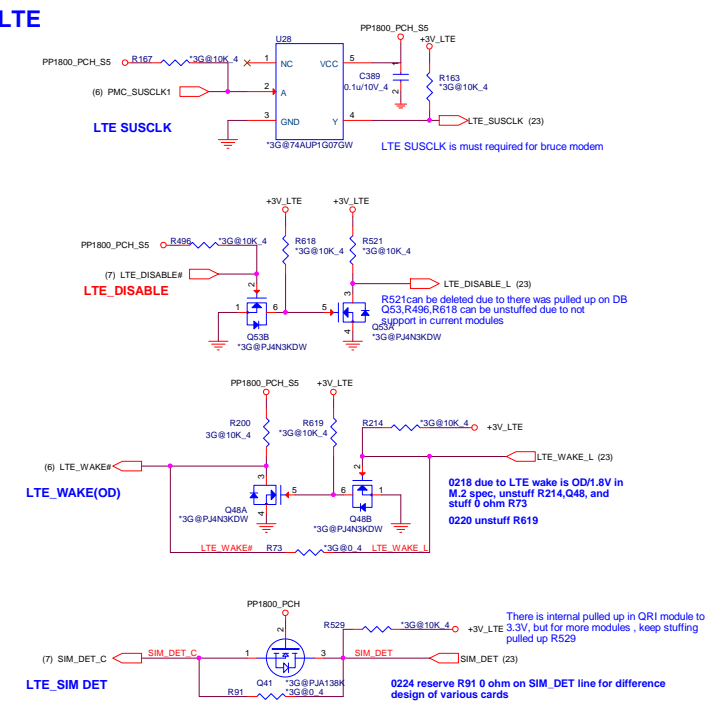
Stuffing for notifying EC

PWRON SEQUENCE



0128 change power rail of
Q35,Q36,Q37,Q44 from PP1800_PCH_S5
to PP1800_PCH for PP1800_PCH
leakage issue in S3 mode

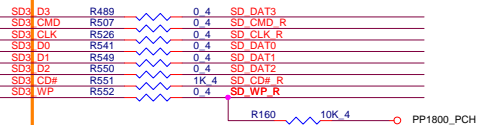
0206 remove/delete SPI_SIO Interface,
Q35,Q36,Q37,Q44,R486,R484,R485,
R483,R426,R429,R427,R428



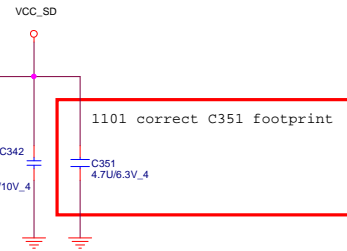
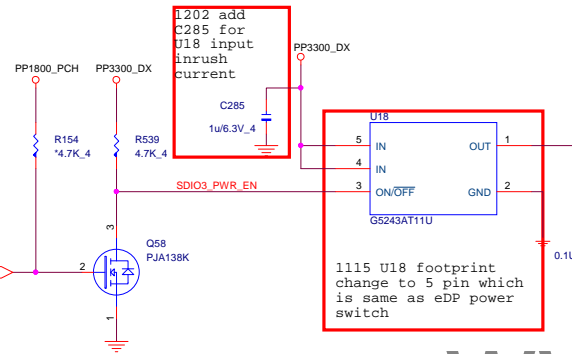
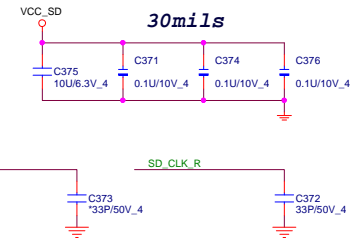
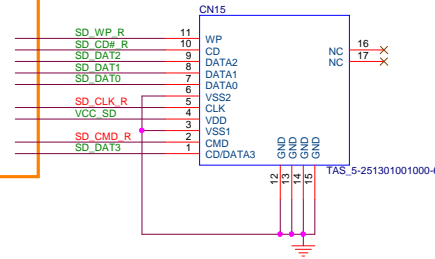
SD/MMC CARD READER CONNECTOR (MMC)

1205 the damping of SDIO change to 0 ohm by Intel request
 1205 add PU for SDIO WP by Intel request
 1205 R551 changes to 1K to isolate SD socket and servo/SoC
 1205 SD3_WP is 1.8V power rail in SoC, change external Pulled up power well of SD3_WP to 1.8V power

(5) SD3_D3
 (5) SD3_CMD
 (5) SD3_CLK
 (5) SD3_D0
 (5) SD3_D1
 (5) SD3_D2
 (5,18) SD3_CD#
 (5) SD3_WP

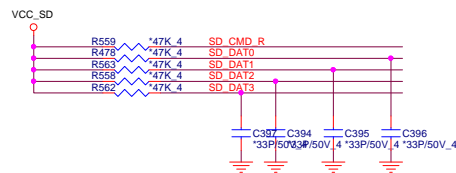


This is full size SD card



1115 U18 footprint change to 5 pin which is same as eDP power switch

1211 add pulled up resistors on SDIO data/cmd lines
 1212 all pulled up resistors of SDIO data/cmd to be un-stuffed



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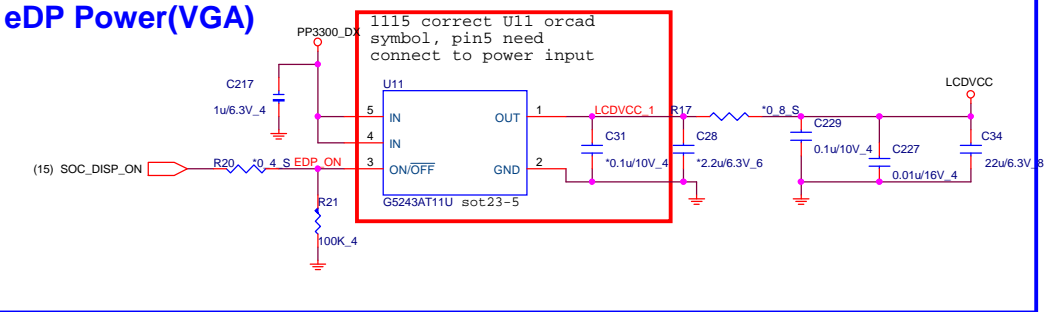
Quanta Computer Inc.

PROJECT : NL6

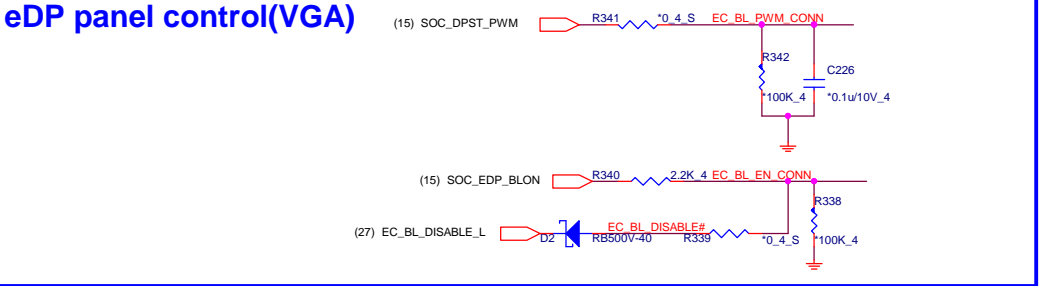
SDIO CardReader

Date: Friday, April 25, 2014 Sheet 16 of 41 Rev 1A

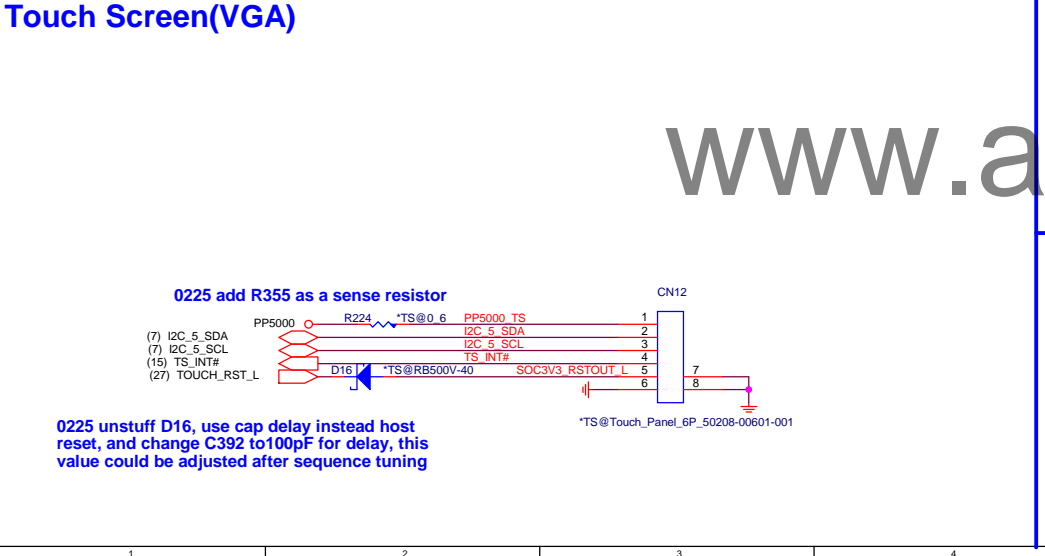
eDP Power(VGA)



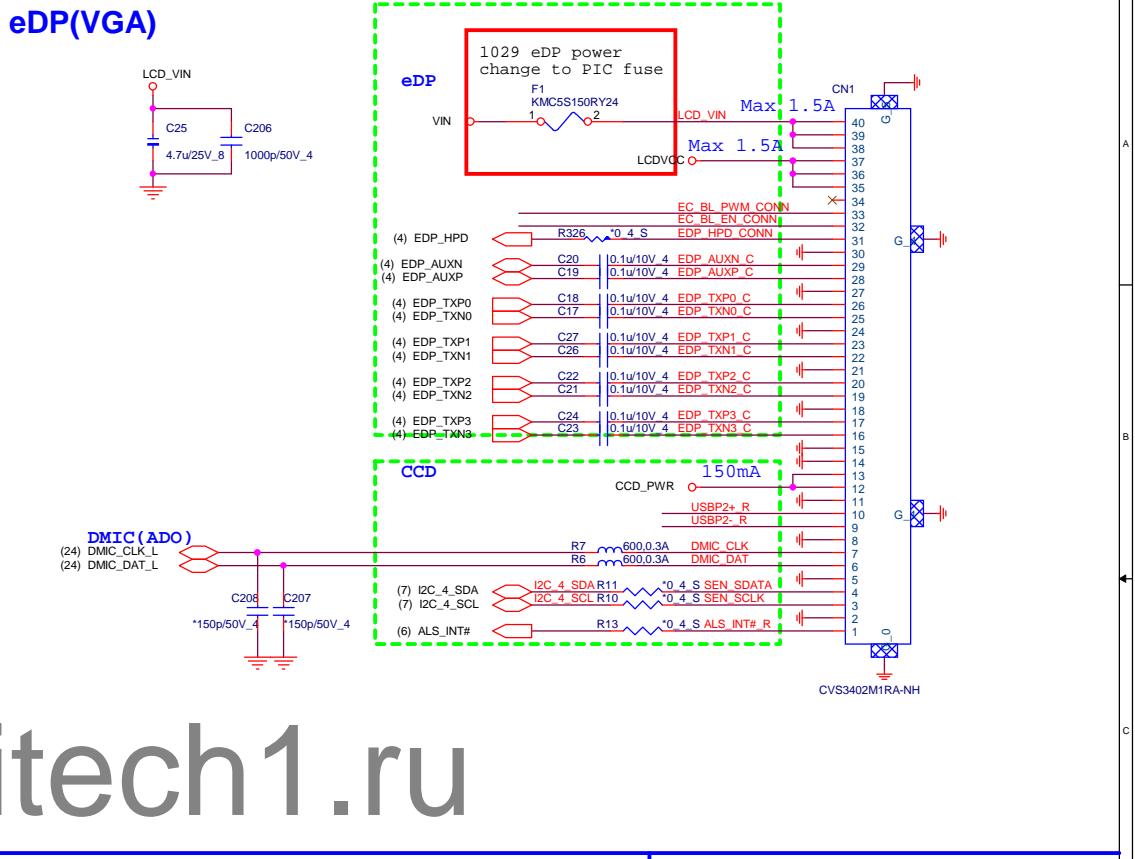
eDP panel control(VGA)



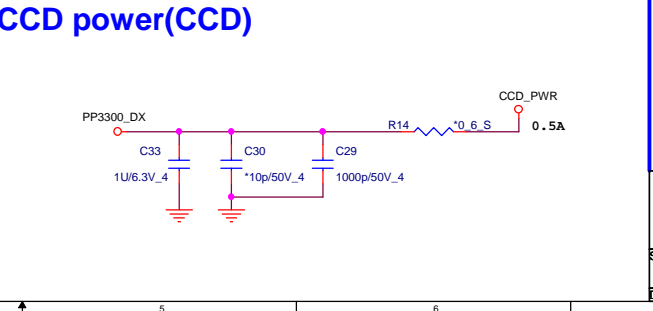
Touch Screen(VGA)



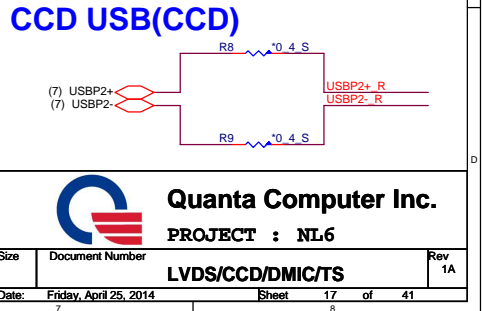
eDP(VGA)



CCD power(CCD)



CCD USB(CCD)



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LVDS/CCD/DMIC/TS

Size Document Number

Date: Friday, April 25, 2014

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Rev 1A

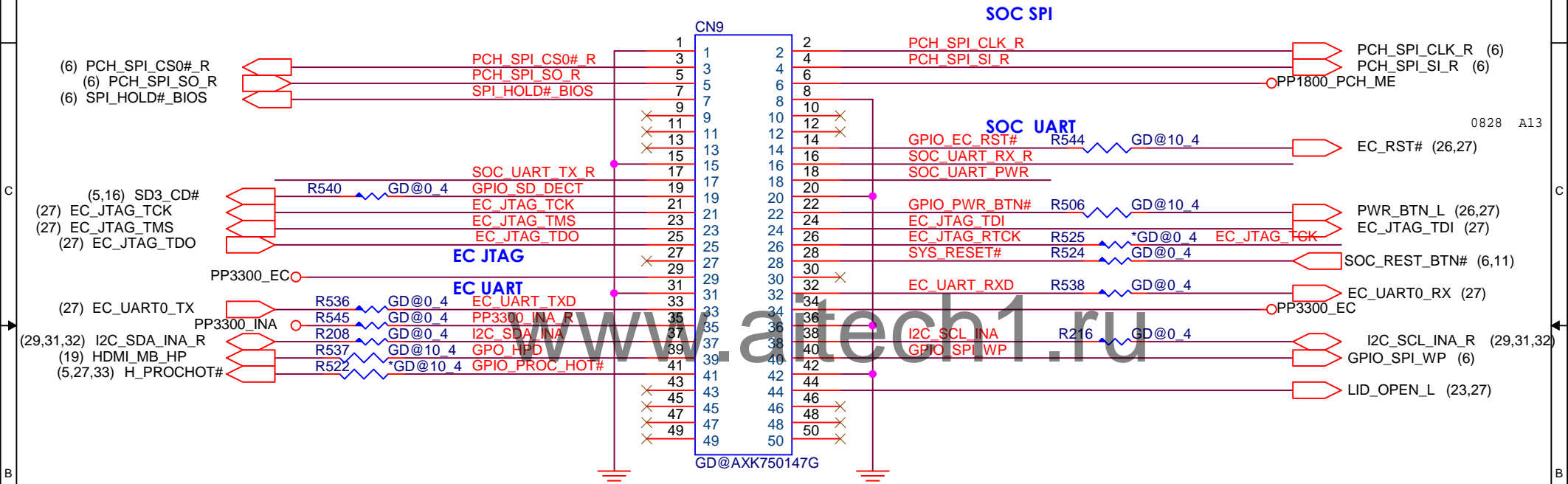
GOOGLE Debug Port(MPC)

50 pin BTB is MUST, don't use 42 pin

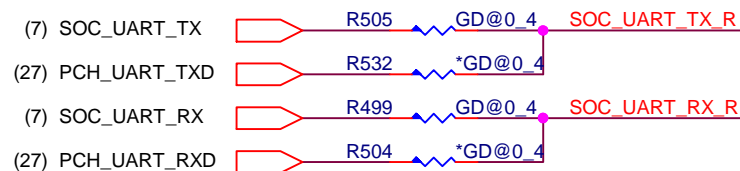
Socket part number AXK750147G

PIN7 OD	PIN39 OD	PIN49 OD
PIN14 OD	PIN41 OD	PIN50 OD
PIN19 OD	PIN43 OD	
PIN22 OD	PIN44 OD	
PIN28 OD	PIN45 OD	
PIN30 OD	PIN46 OD	
PIN37 OD	PIN47 OD	
PIN38 OD	PIN48 OD	

18

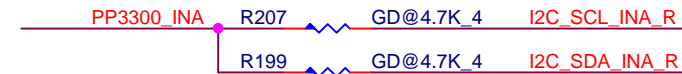


1021 change footprint and PN



9/6 using optional instead of level shifted, default is from SoC

9/13 add pull up

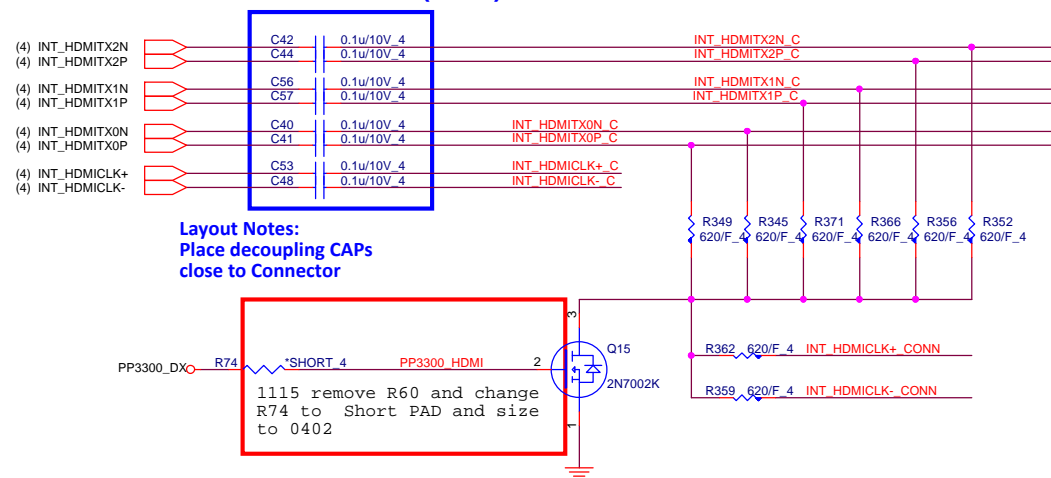


Quanta Computer Inc.

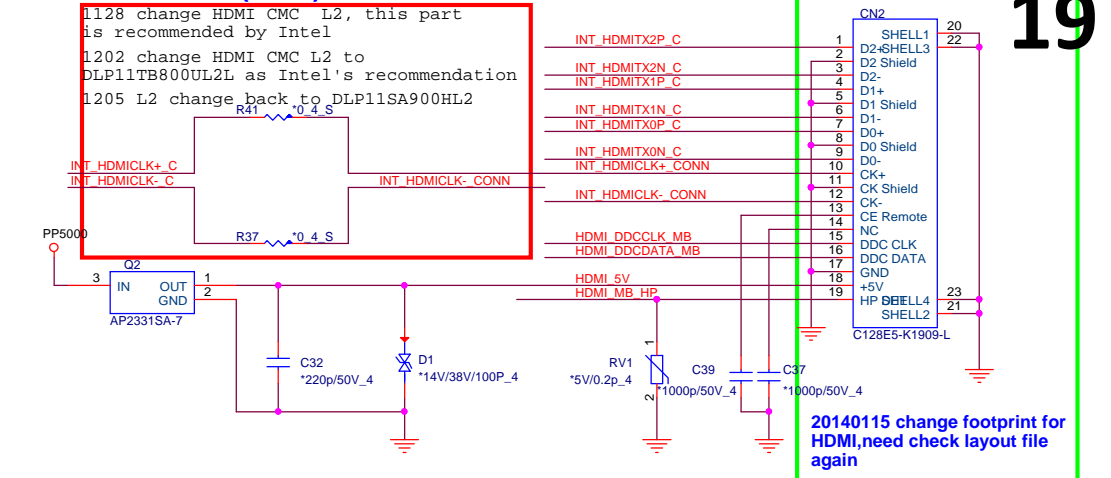
PROJECT : NL6

Size	Document Number	Rev
	Google Debug	1A
Date:	Friday, April 25, 2014	Sheet 18 of 41

HDMI Cost Reduced level shift (HDM)

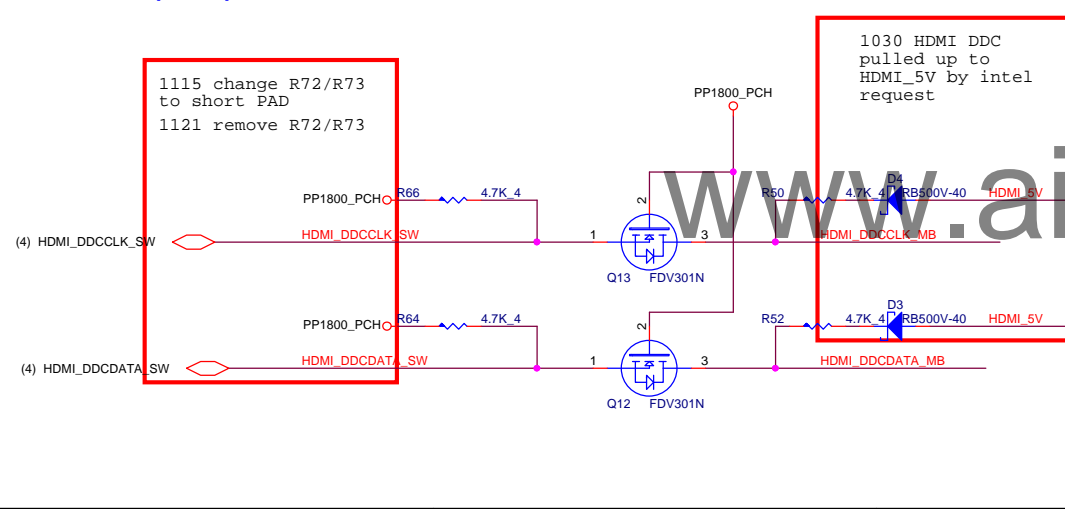


HDMI connector (HDM)

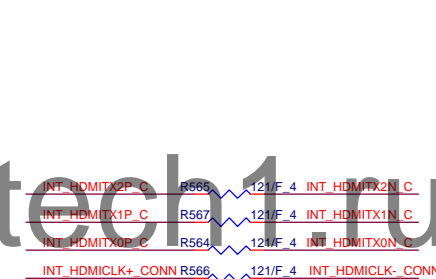


19

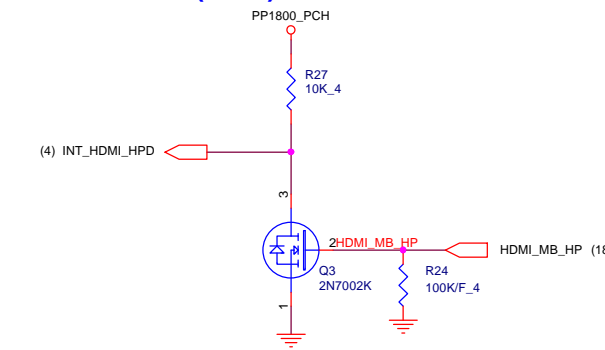
HDMI DDC (HDM)



EMI



HDMI-detect (HDM)



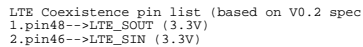
Quanta Computer Inc.

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HDMI

Size Document Number Rev 1A

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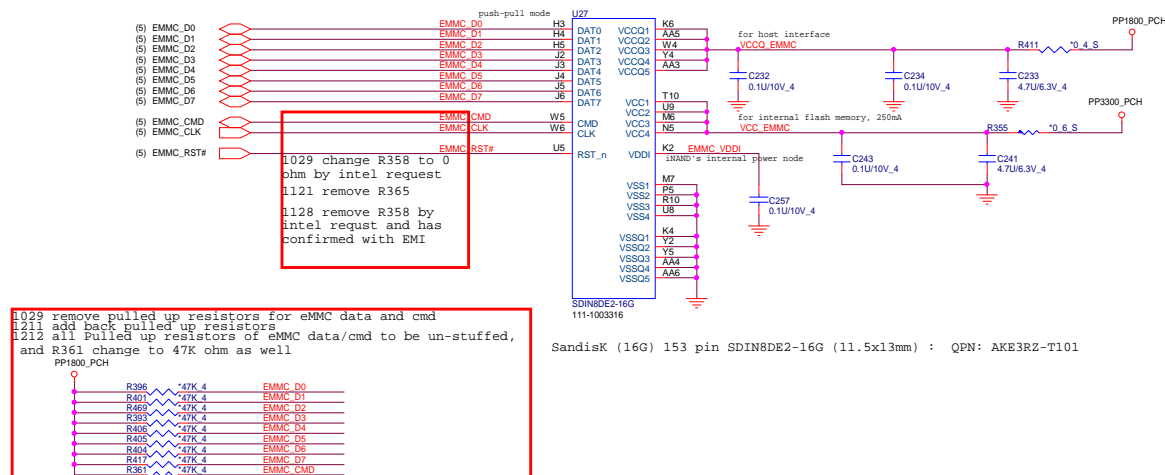
www.aitech1.ru

[illegible]

1025 Delete complete SSD(connector and caps)

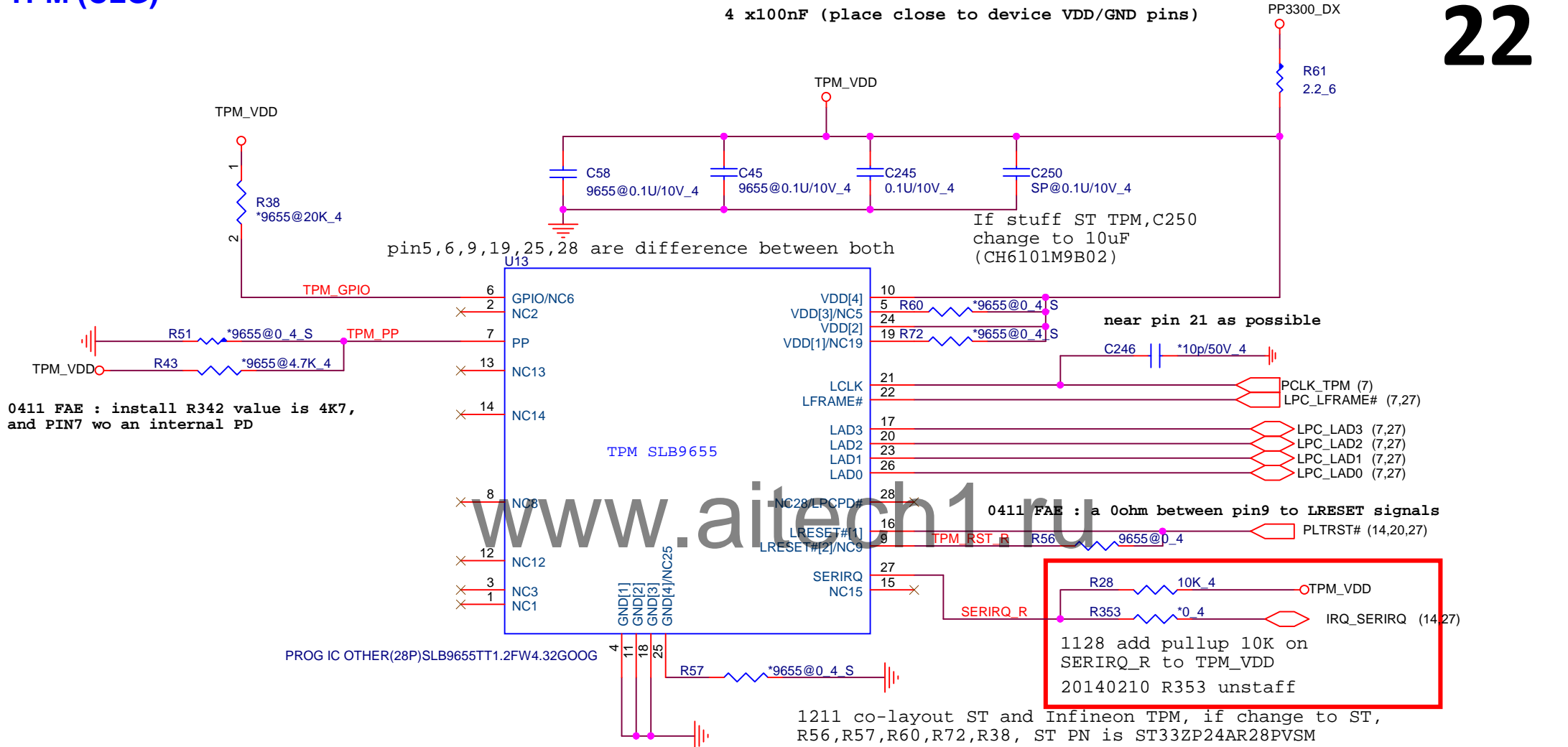
www.aitech1.ru

EMMC (CBS)

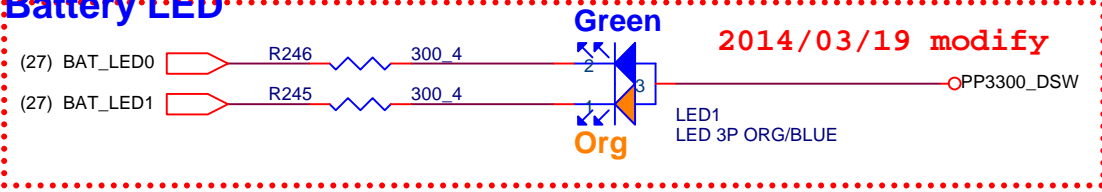


TPM (CLG)


22



LED(UIF) Battery LED



0319 Del Power LED

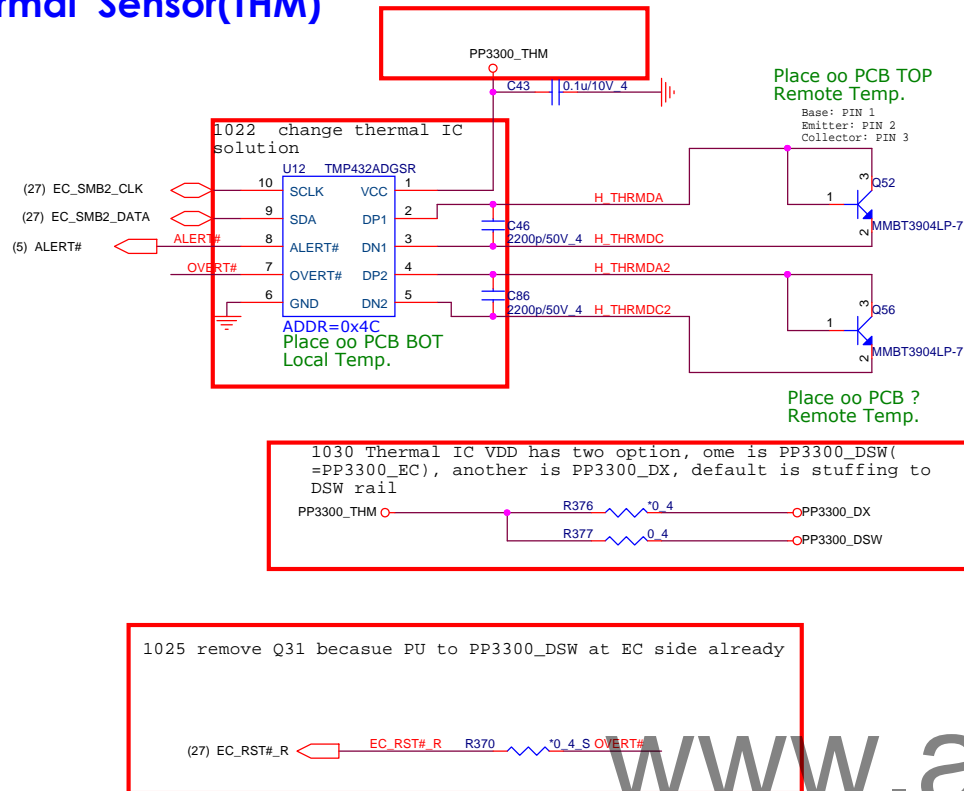


Quanta Computer Inc.

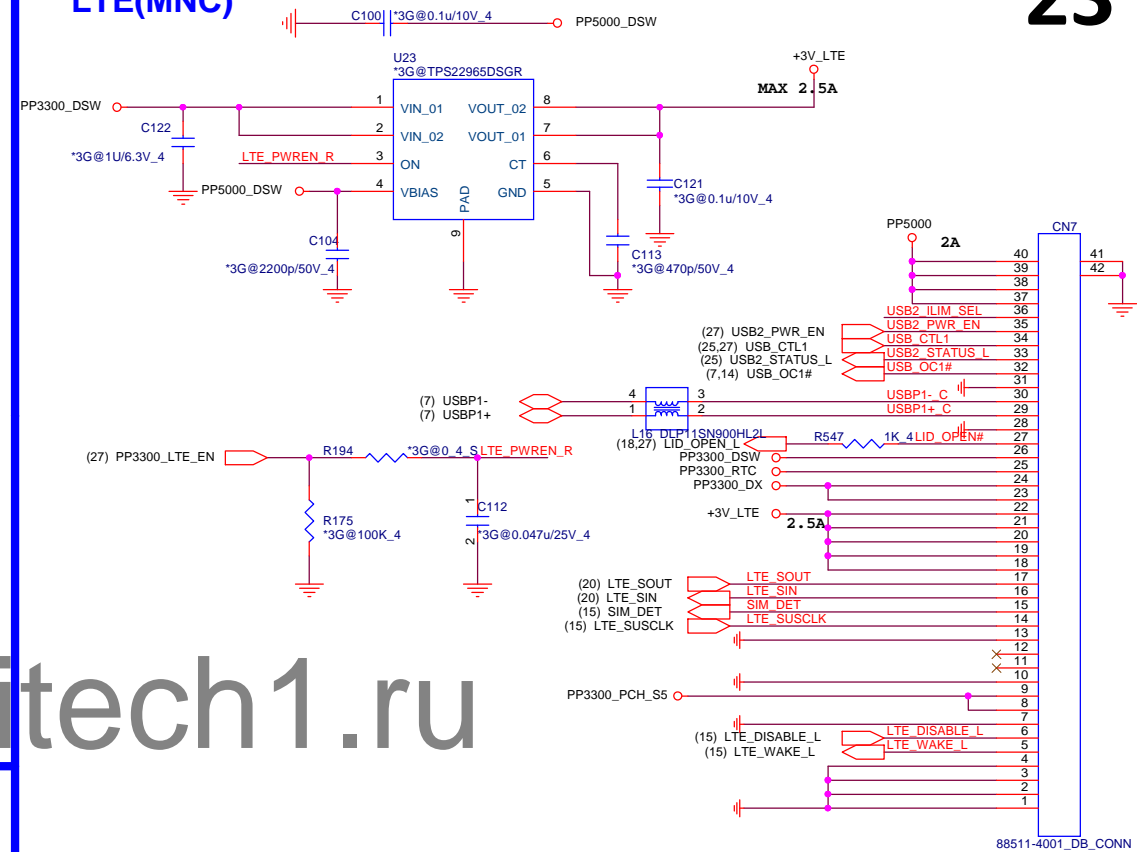
PROJECT : NL6

Size	Document Number	Rev
	TPM SLB9655 / LED	1A
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Thermal Sensor(THM)

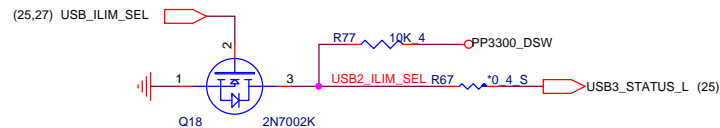



FUNCTION DB LTE(MNC)



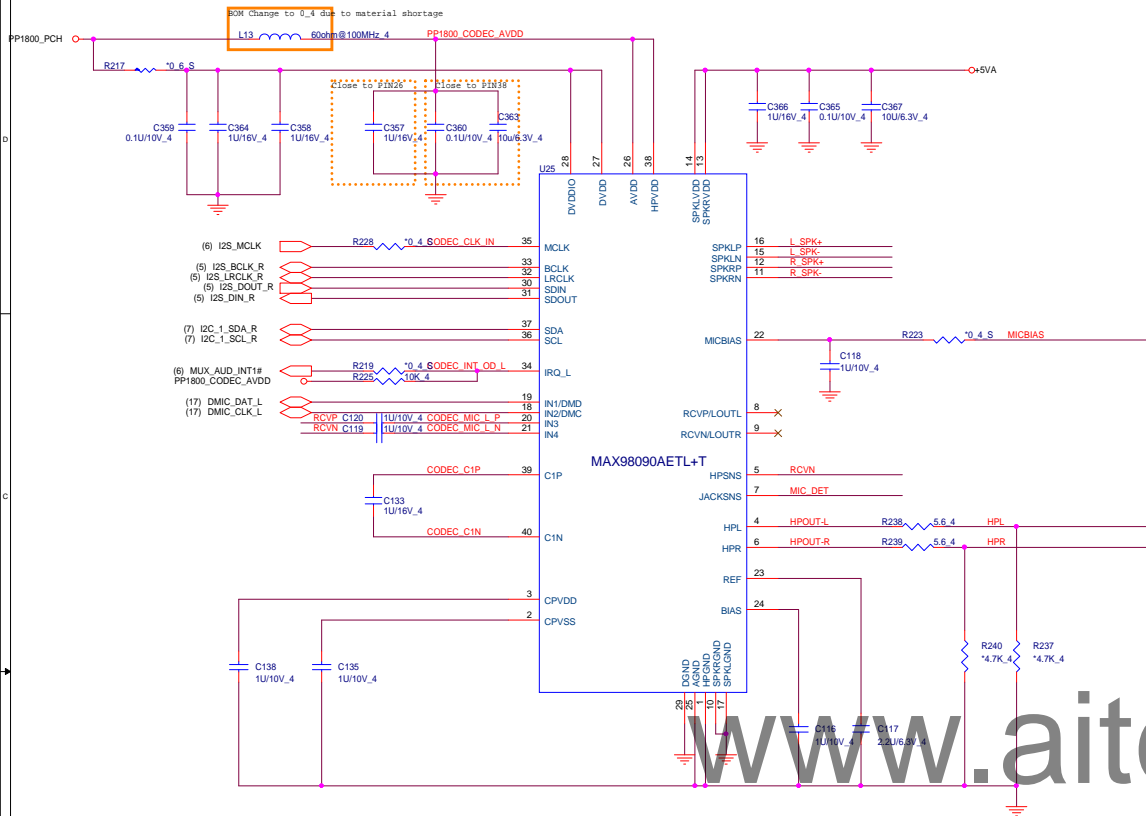
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USB Switch Current Control

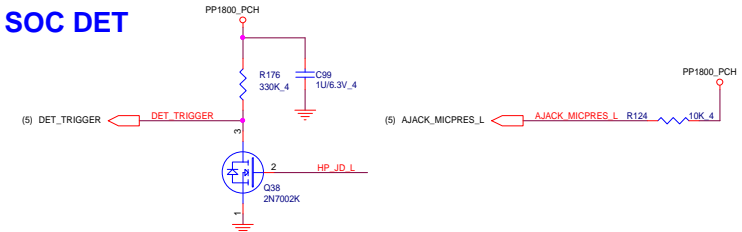


 Quanta Computer Inc. PROJECT : NL6		Size	Document Number	Rev
			DB/ALS/Thermal sensor	1A
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AUDIO CODEC (ADO)



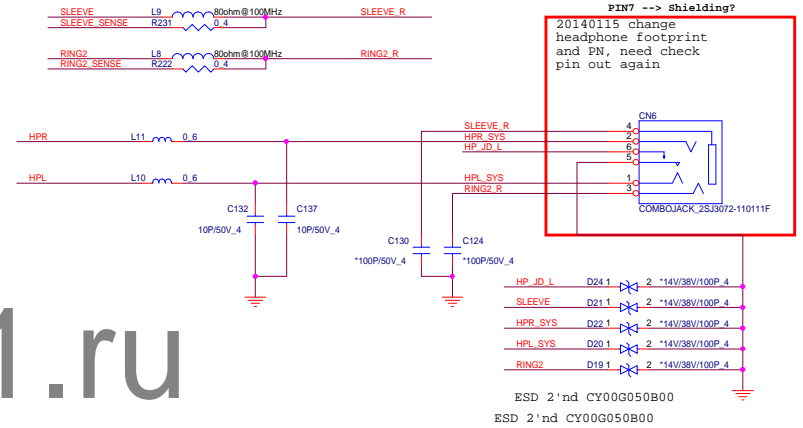
SOC DET



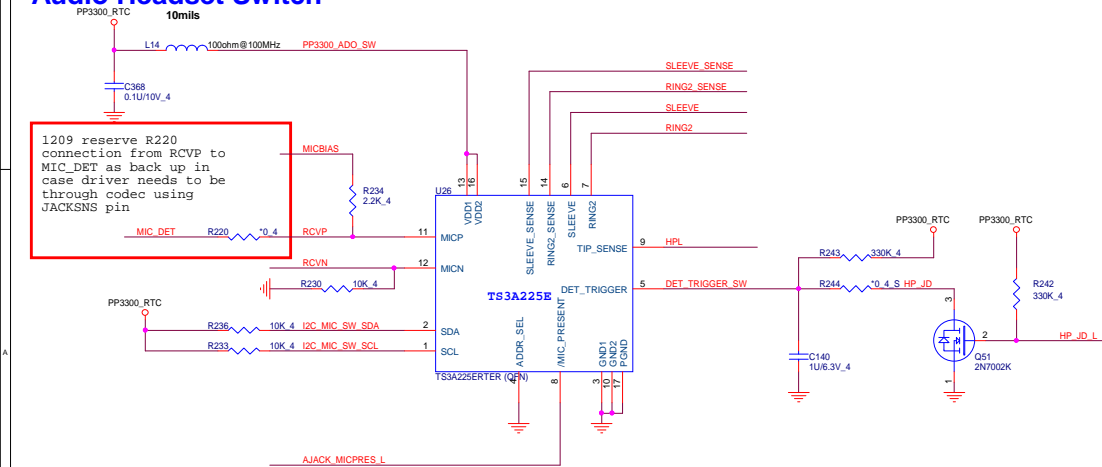
HEADPHONE/Mic combo(ADO)

combo jack
Normal open

P/N: DFTJ06FR652
Normal Open
PIN1 --> L?
PIN2 --> R?
PIN3 --> GND/MIC?
PIN4 --> MIC/GND?
PIN5 --> JD?
PIN6 --> GND?
PIN7 --> Shielding?

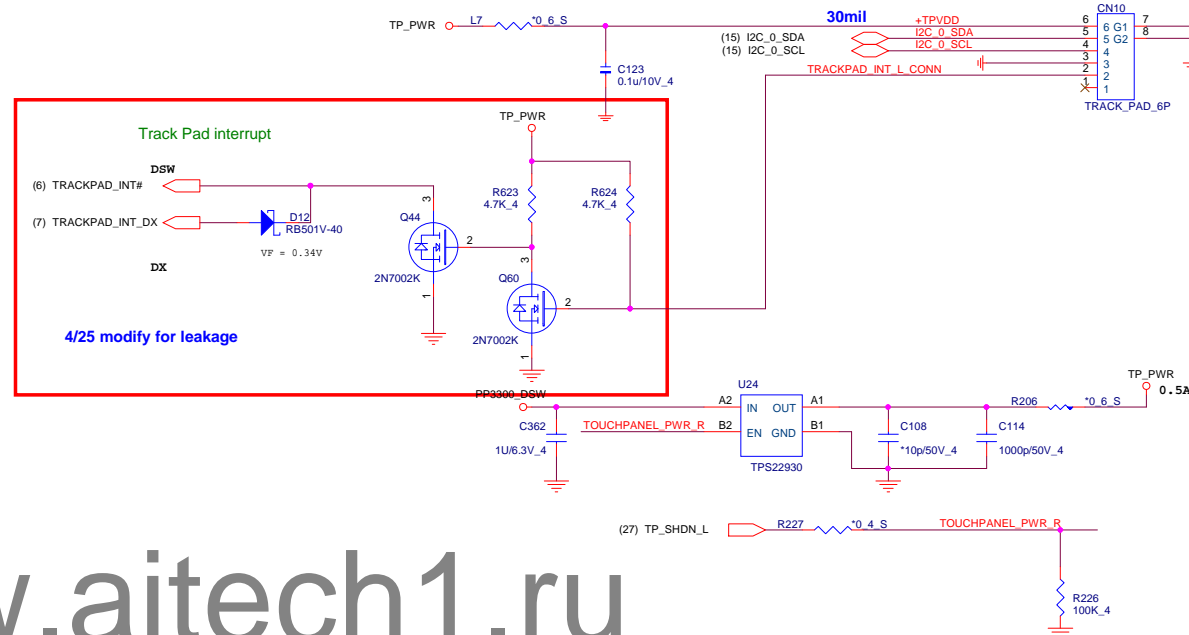
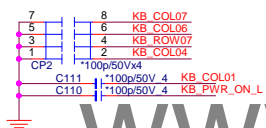
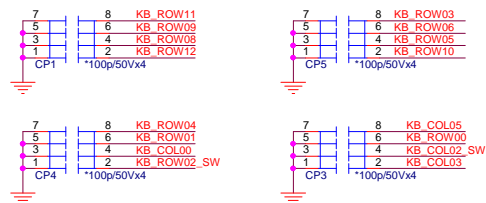
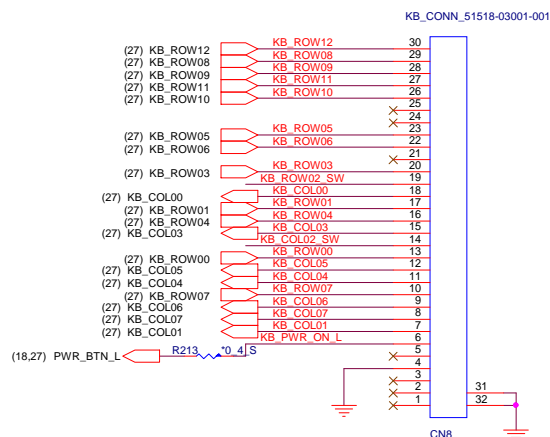


Audio Headset Switch



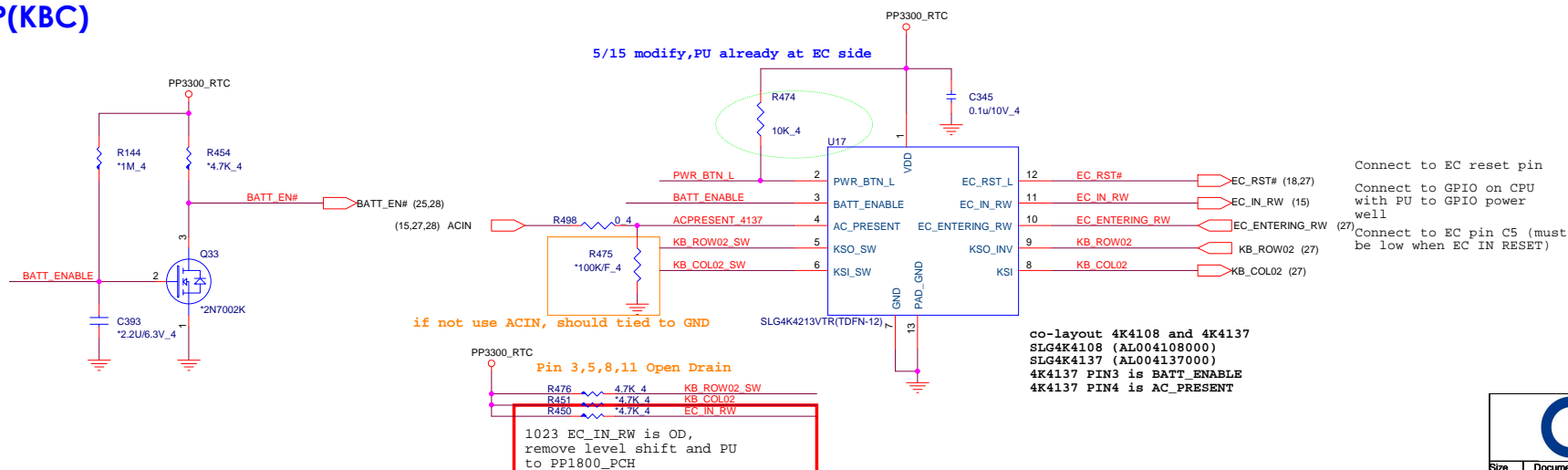
Track PAD BOARD CONN (TPD)

20140127 Change KB CONN for ME require



10 | ["100p/50V 4 KB COL01](#)
["100p/50V 4 KB PWR_ON_L](#)

HOLELESS RESET 2-CHIP(KBC)

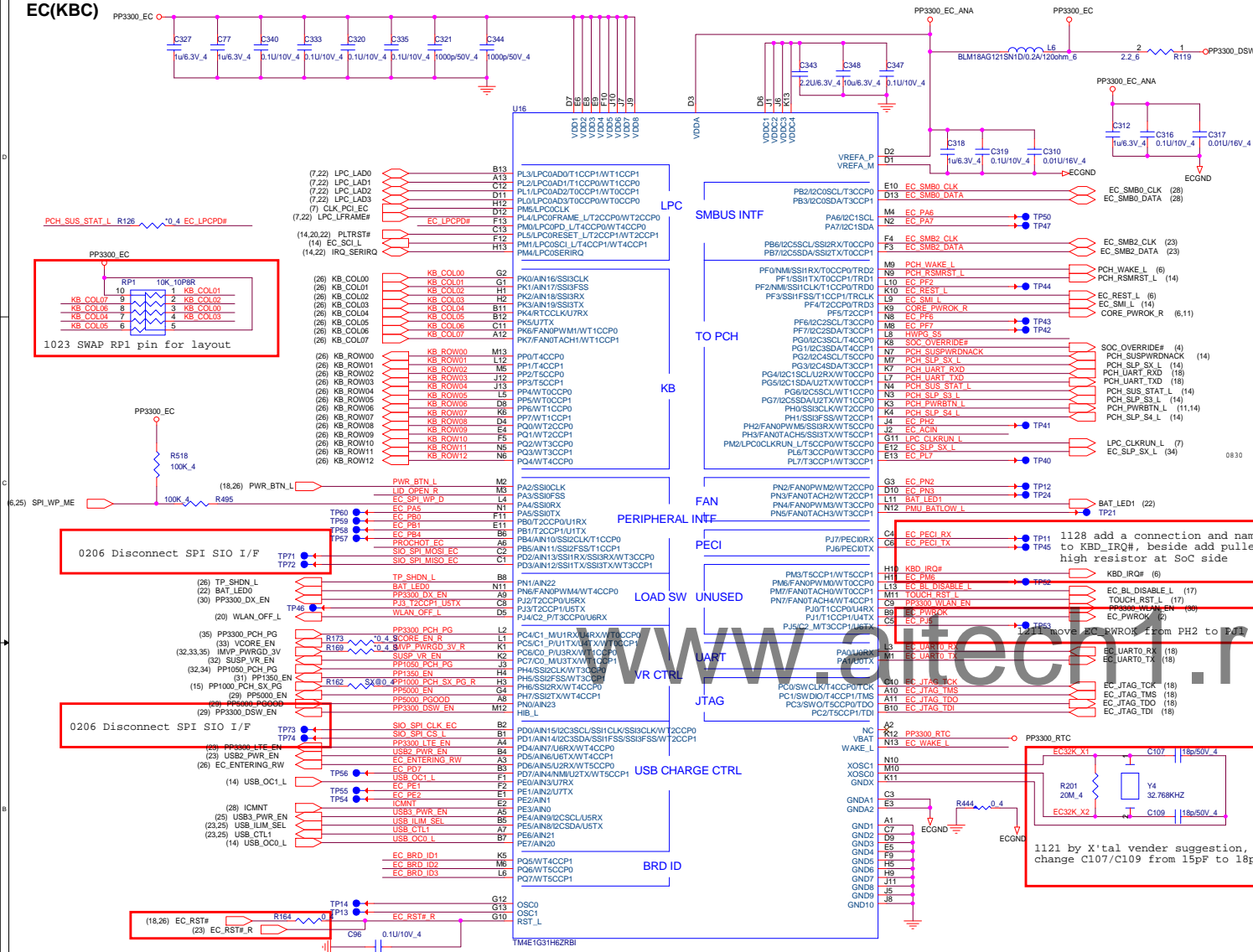


```
co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT
```

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Size	Document Number	Rev
	KB/TP/FAN/HW Reset	1A
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Add diode for leakage issue



(15,26,28) ACIN



SM BUS/I2C PU(KBC)

BATT and CHARGER / LCD BL

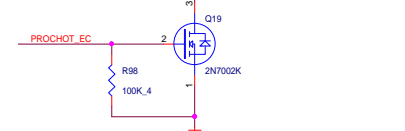


1030 Thermal IC VDD has two option, one is PP3300_DSW(=PP3300_EC), another is PP3300_DX, default is stuffing to DSW rail

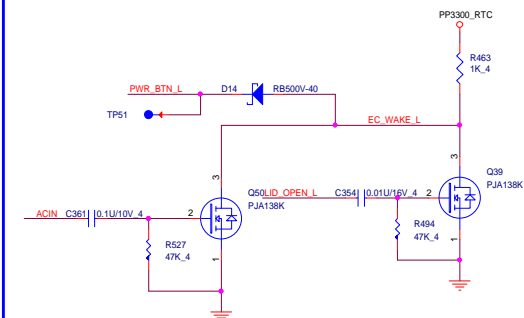
THERMAL SENSOR



H_PROCHOT# (5,18,33)



EC HIB WAKE SOURCES



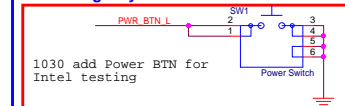
SM BUS ARRANGEMENT TABLE

SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

OD pin list

EC_REST_L
BAT_LED0
BAT_LED1
PCH_RSMRST_L
SMBUS
IRQ_SERIRQ
EC_BL_DISABLE_L

For testing only

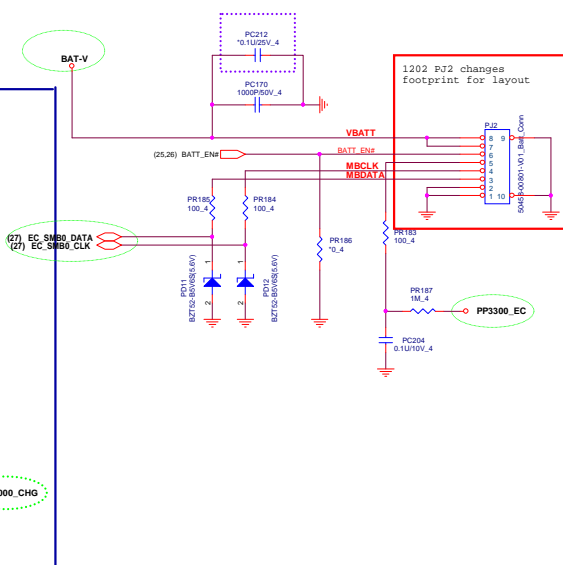
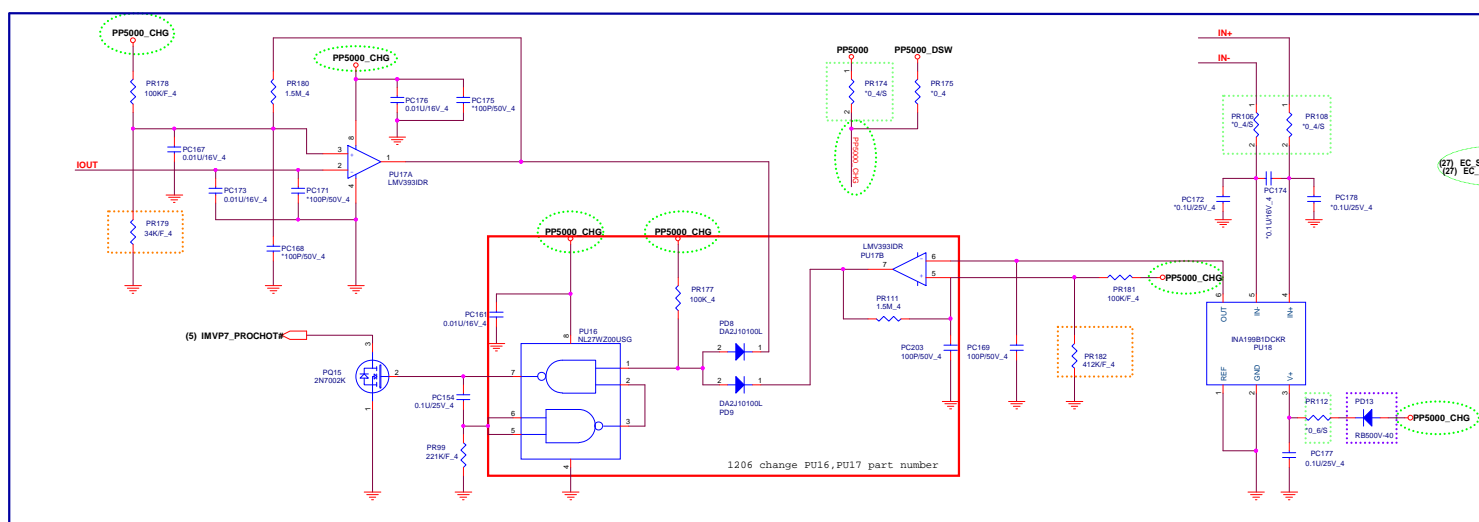
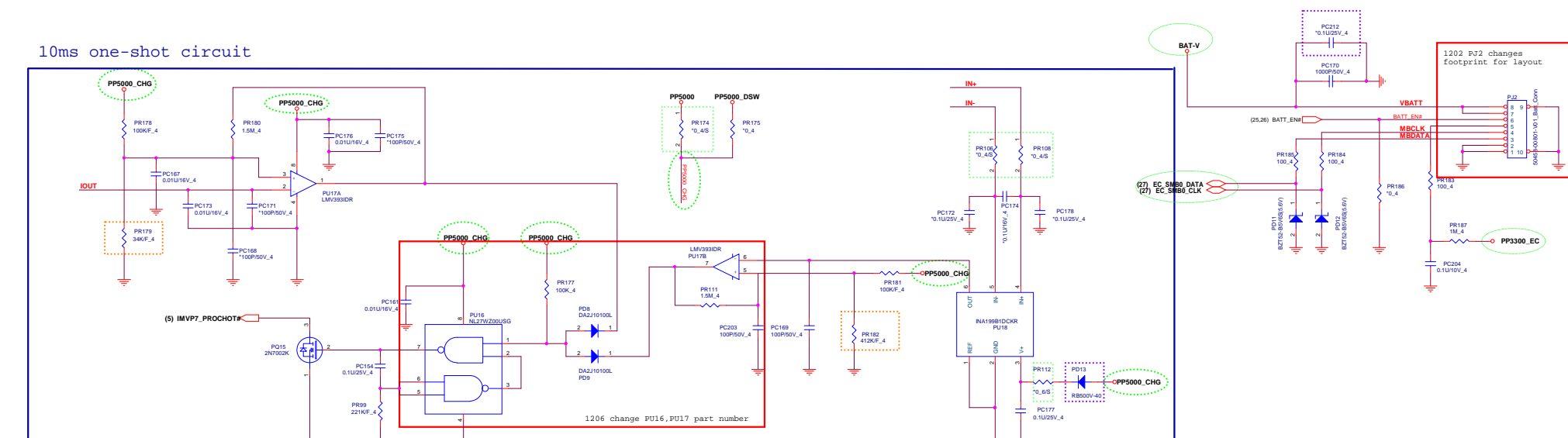


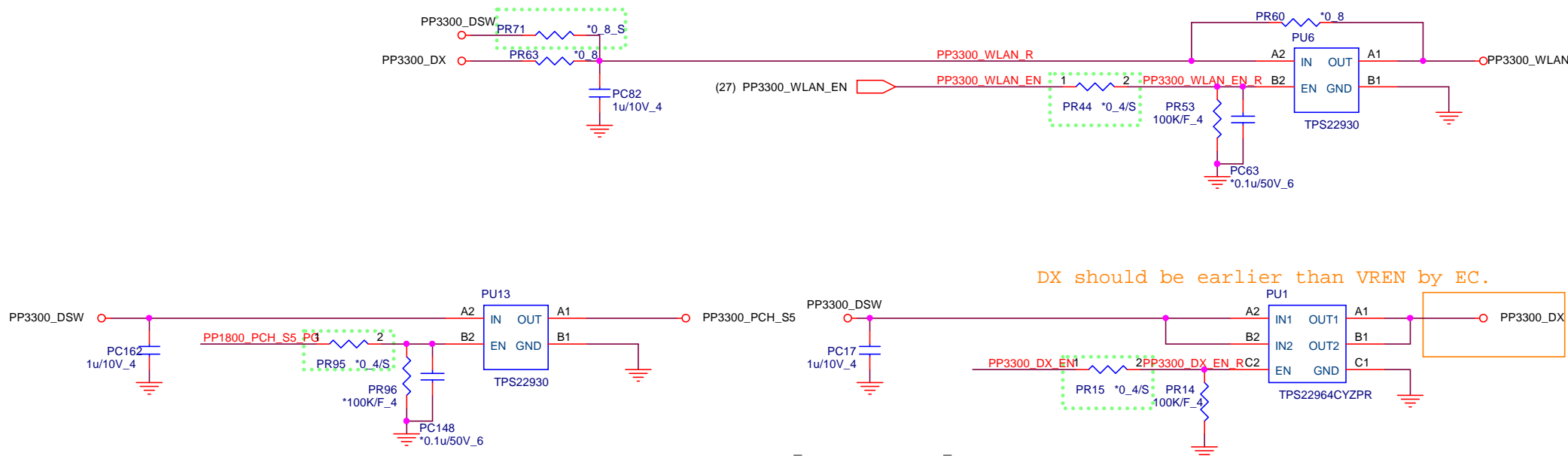
1030 add Power BTN for Intel testing

Quanta Computer Inc.
PROJECT : NL6

Size Document Number KBC TI TM4E1G31H6ZRB1 Rev 1A

Date: Friday, April 25, 2014 Sheet 27 of 41





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**Quanta Computer Inc.**

PROJECT :

Size	Document Number Load Switch	Rev 1A
Date:	Friday, April 25, 2014	Sheet 30 of 40

TDC : 0.75A
PEAK : 1A
Width : 10mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

Greater than or equal 40mil

0417 PC13 change to 10uF ,
add 2x10uF PC215 , PC216

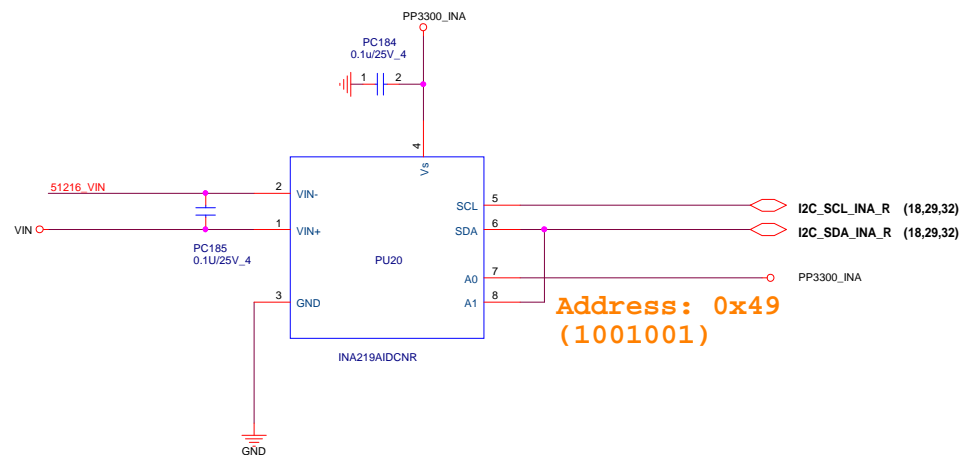
1.35 Volt +/- 5%
TDC : 3.55A
PEAK : 4.73A
OCP : 6A
Width : 160mil

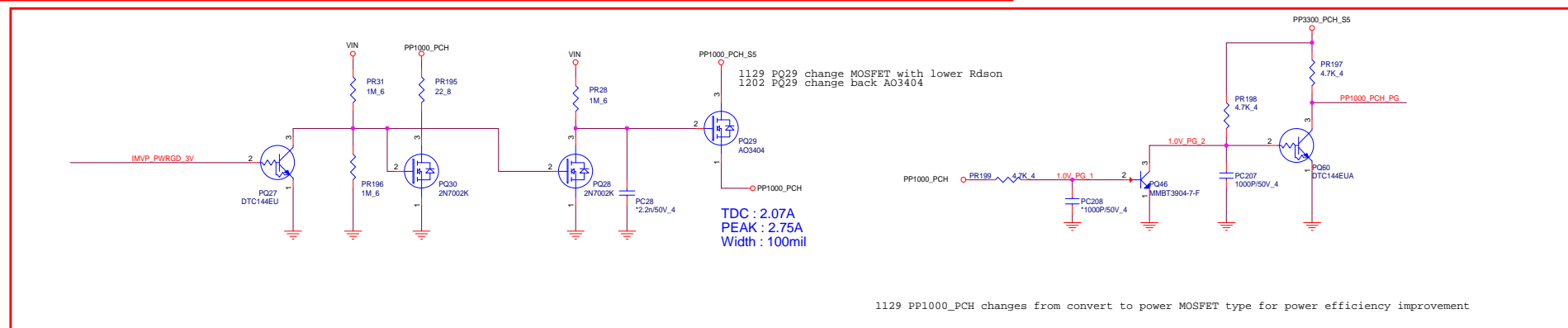
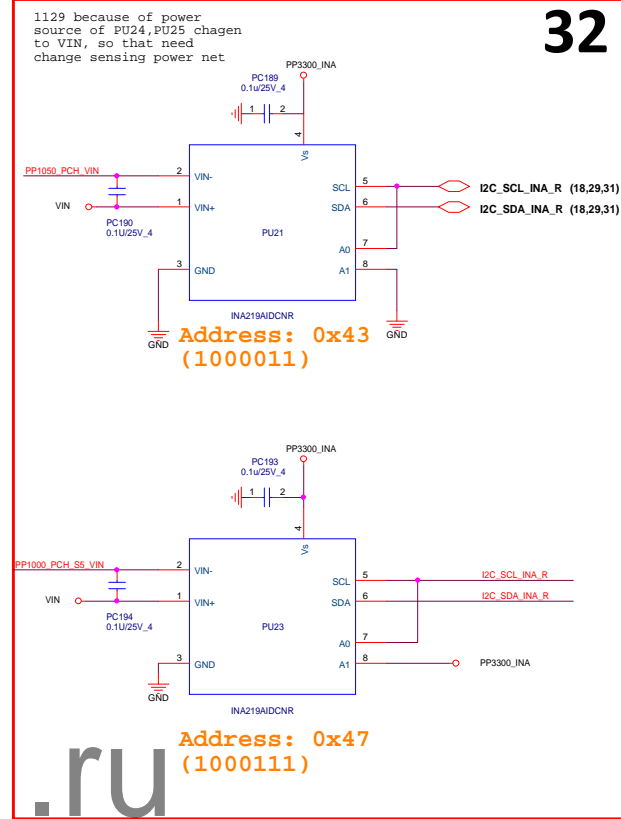
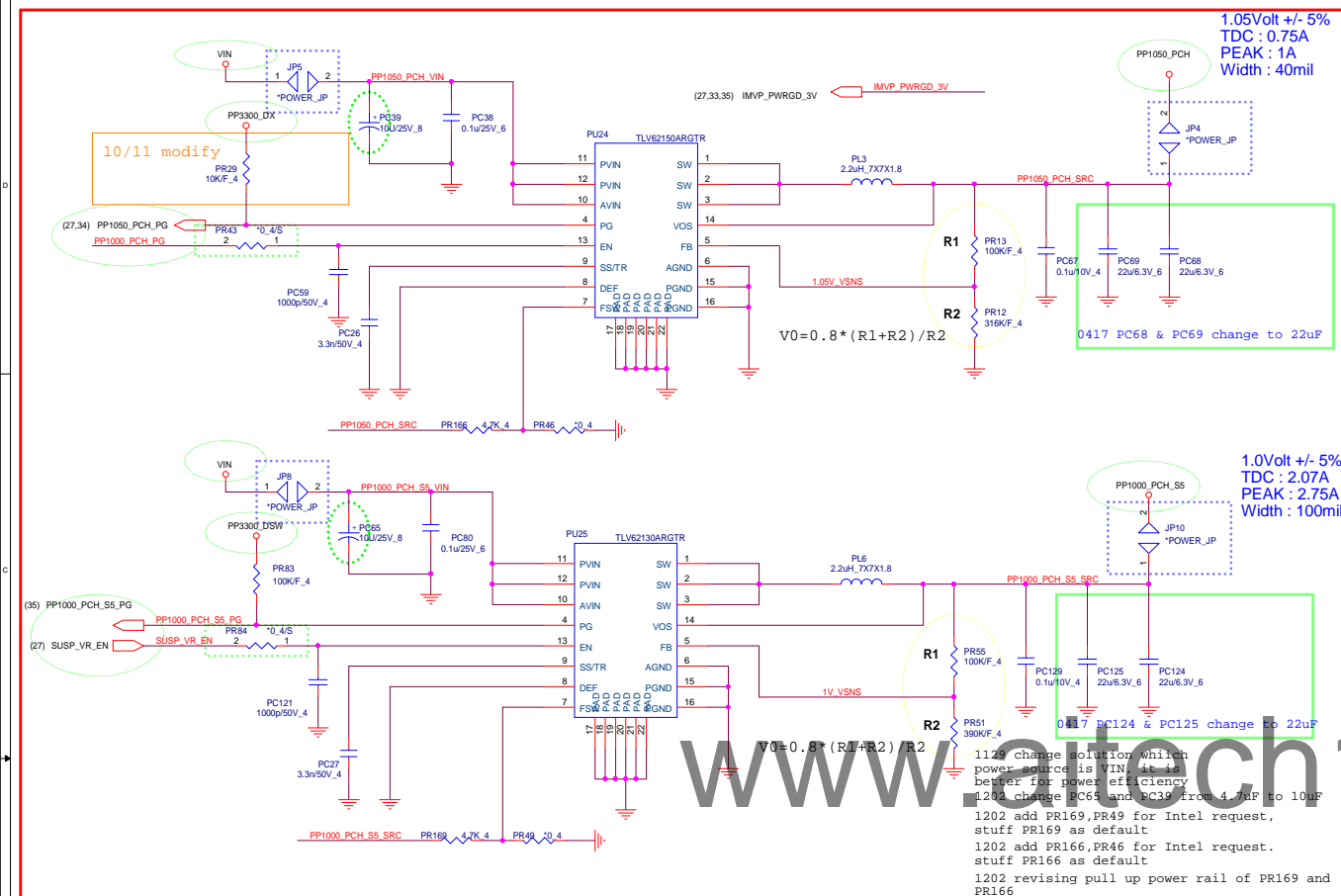
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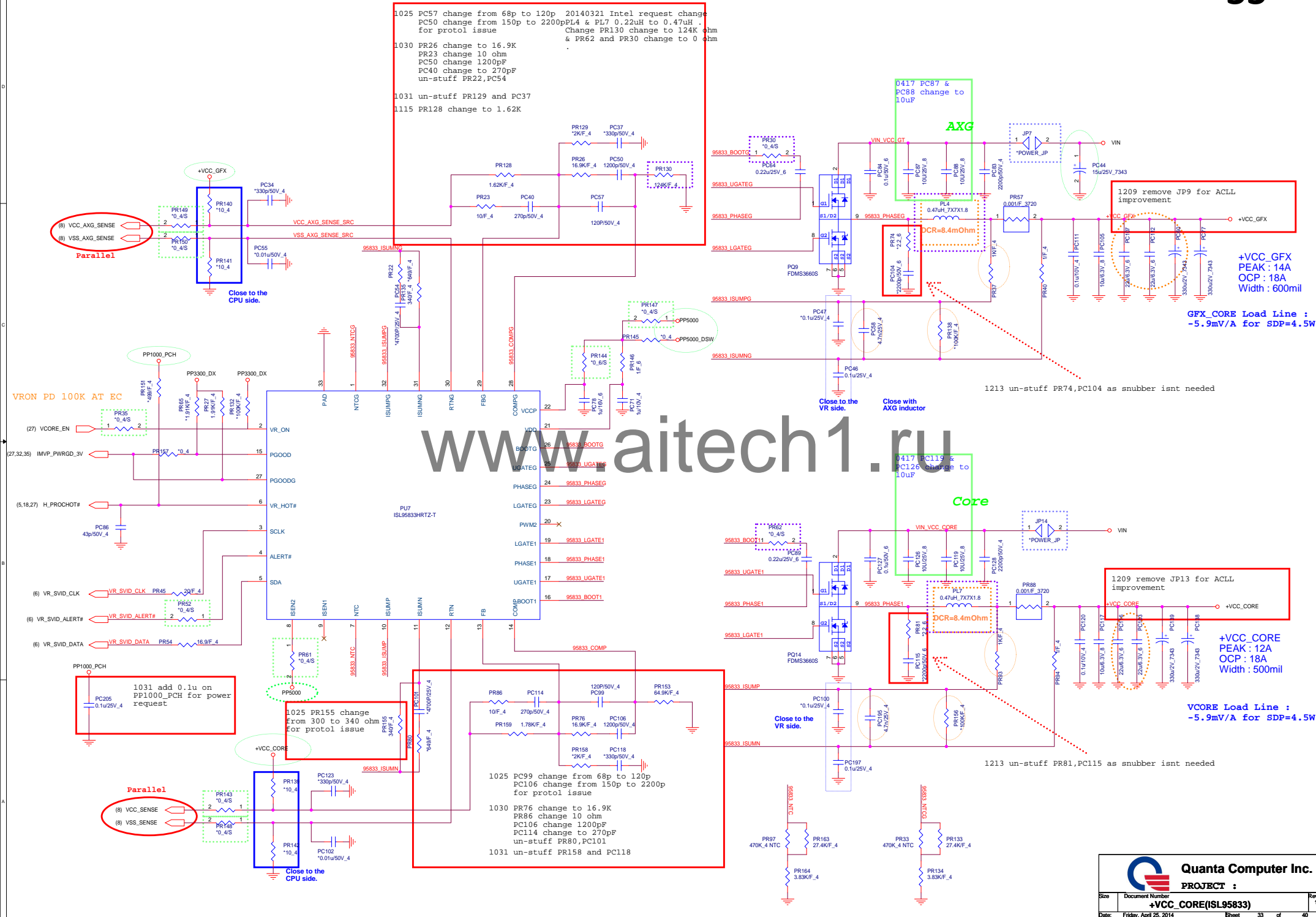
OCP=6A
L ripple current
= $(19-1.35) \times 1.35 / (2.2 \times 400 \times 19)$
=1.425A
 $V_{trip} = [6 - (1.425/2)] \times 14 \text{mohm}$
=0.07402V
 $R_{limit} = 0.07402 / 10 \mu A \times 8 = 59.22 \text{Kohm}$

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

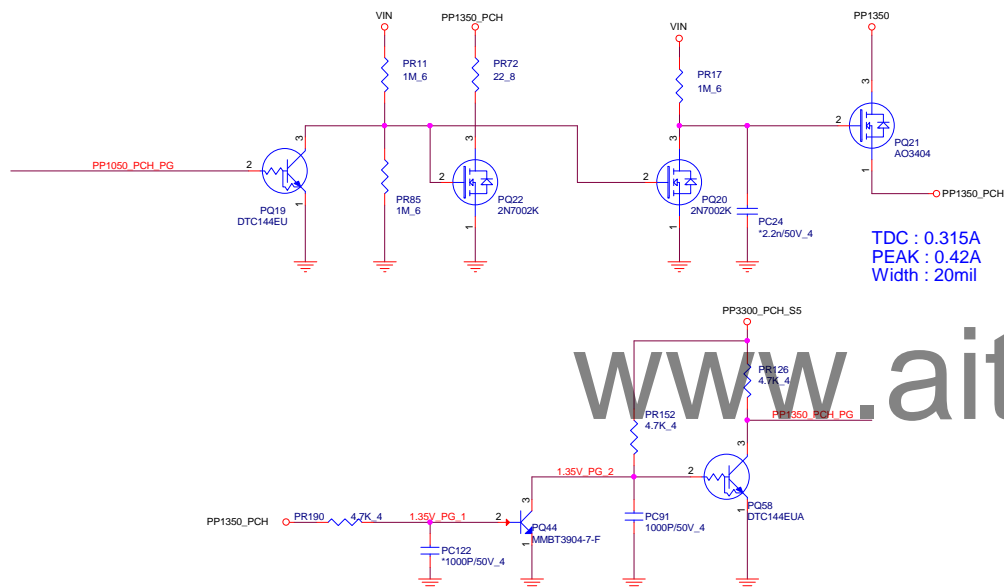
	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



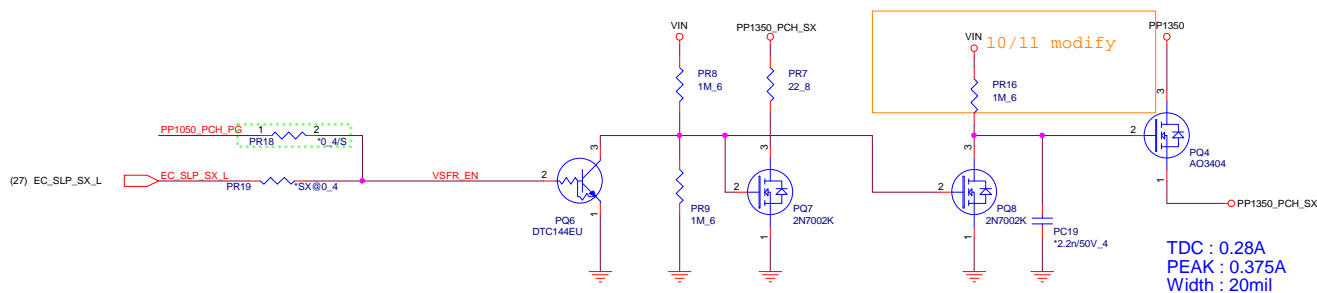




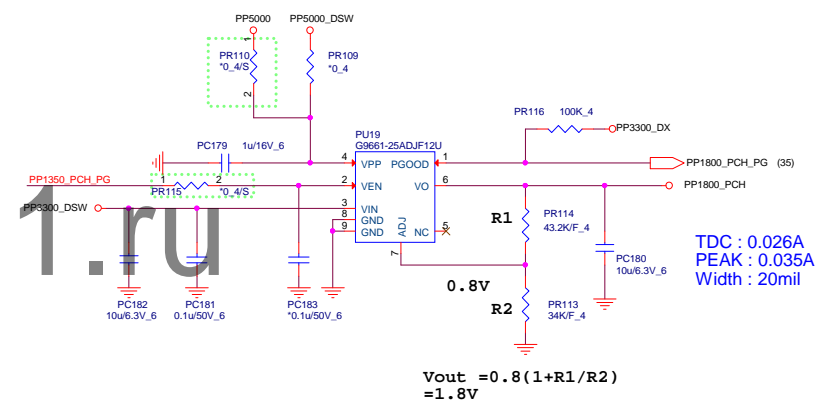
1129 PP1000_PCH_S5 change from LDO to switching power

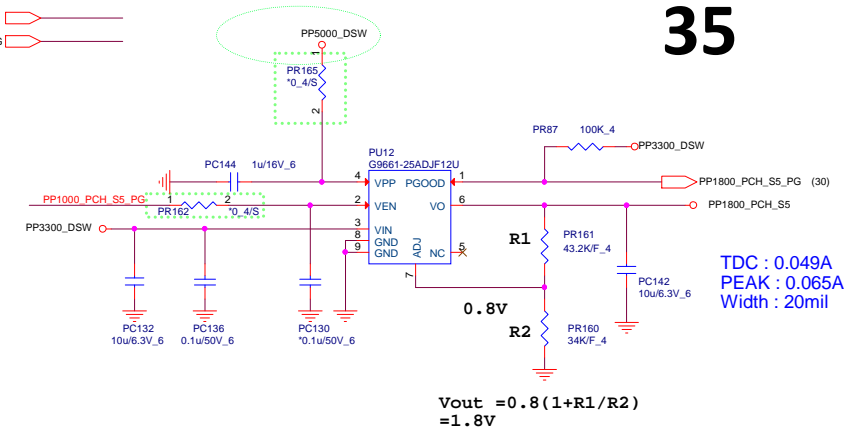


1129 PP1350_PCH change from LDO to power MOSFET



(31) VSFR_EN
(27,32) SUSP_VR_EN
(27,32) PP1050_PCH_PG

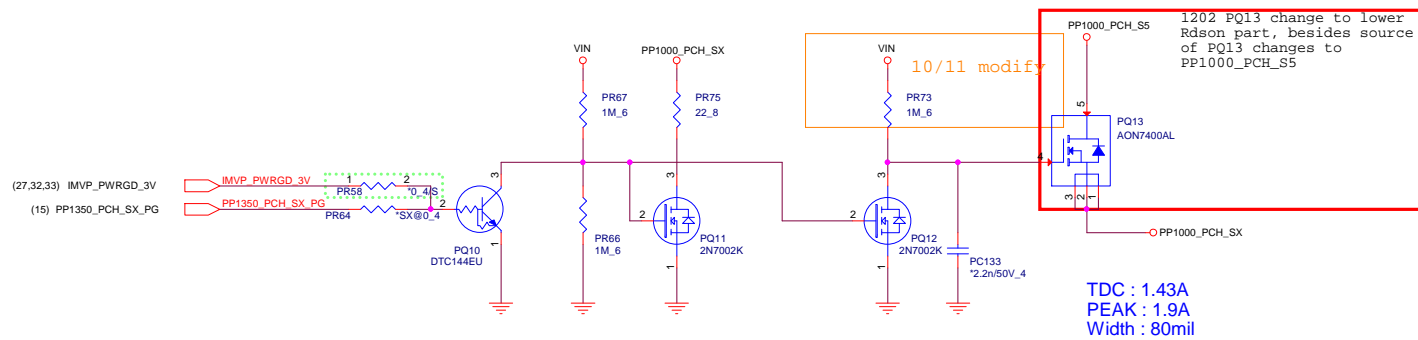




TDC : 0.025A
PEAK : 0.033A
Width : 20mil

1213 change pull up power
of PP3300_PCH_PG to
PP3300_EC

1129 PP3300_PCH change from LDO to power MOSFET



TDC : 1.43A
PEAK : 1.9A
Width : 80mil

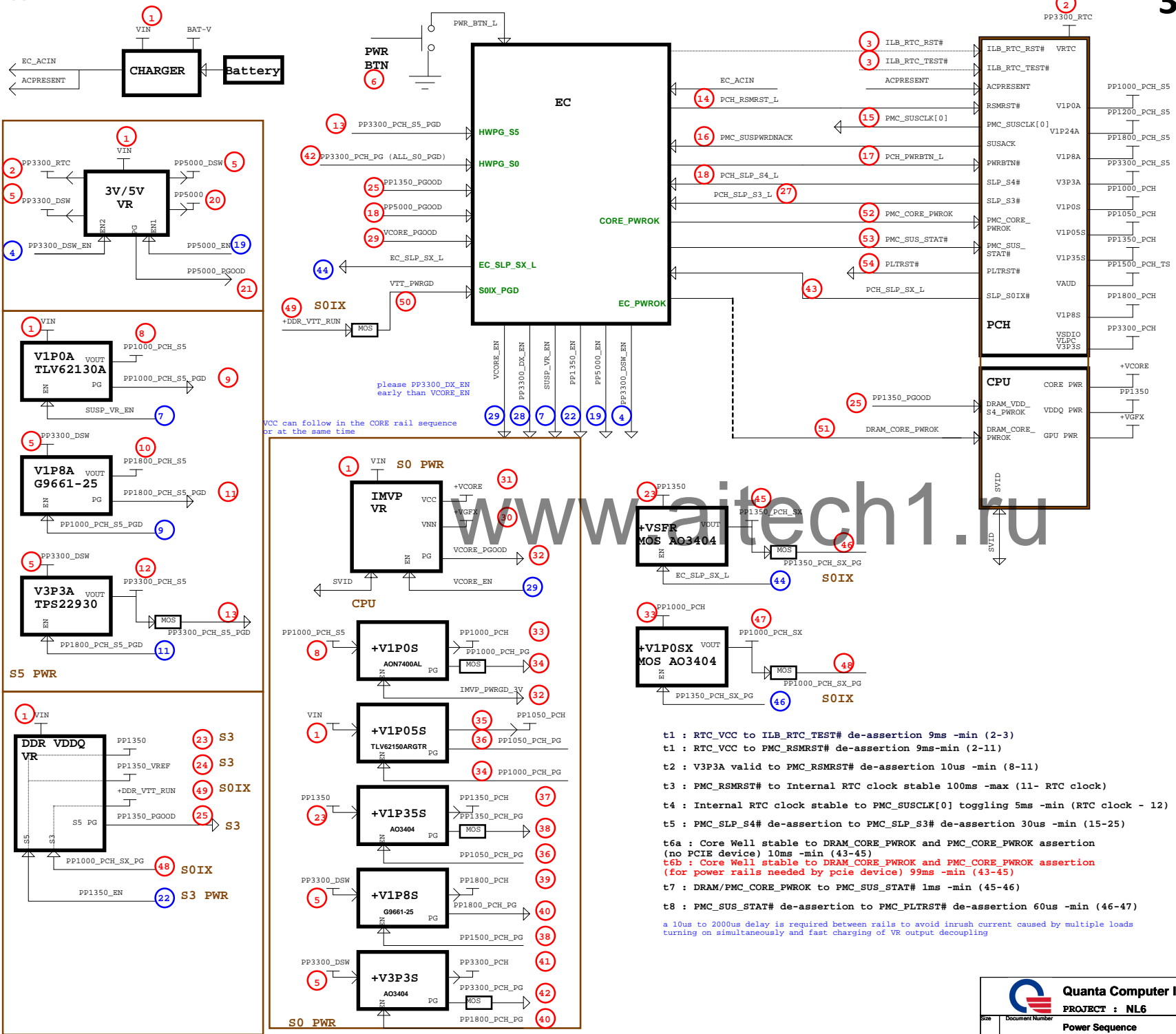
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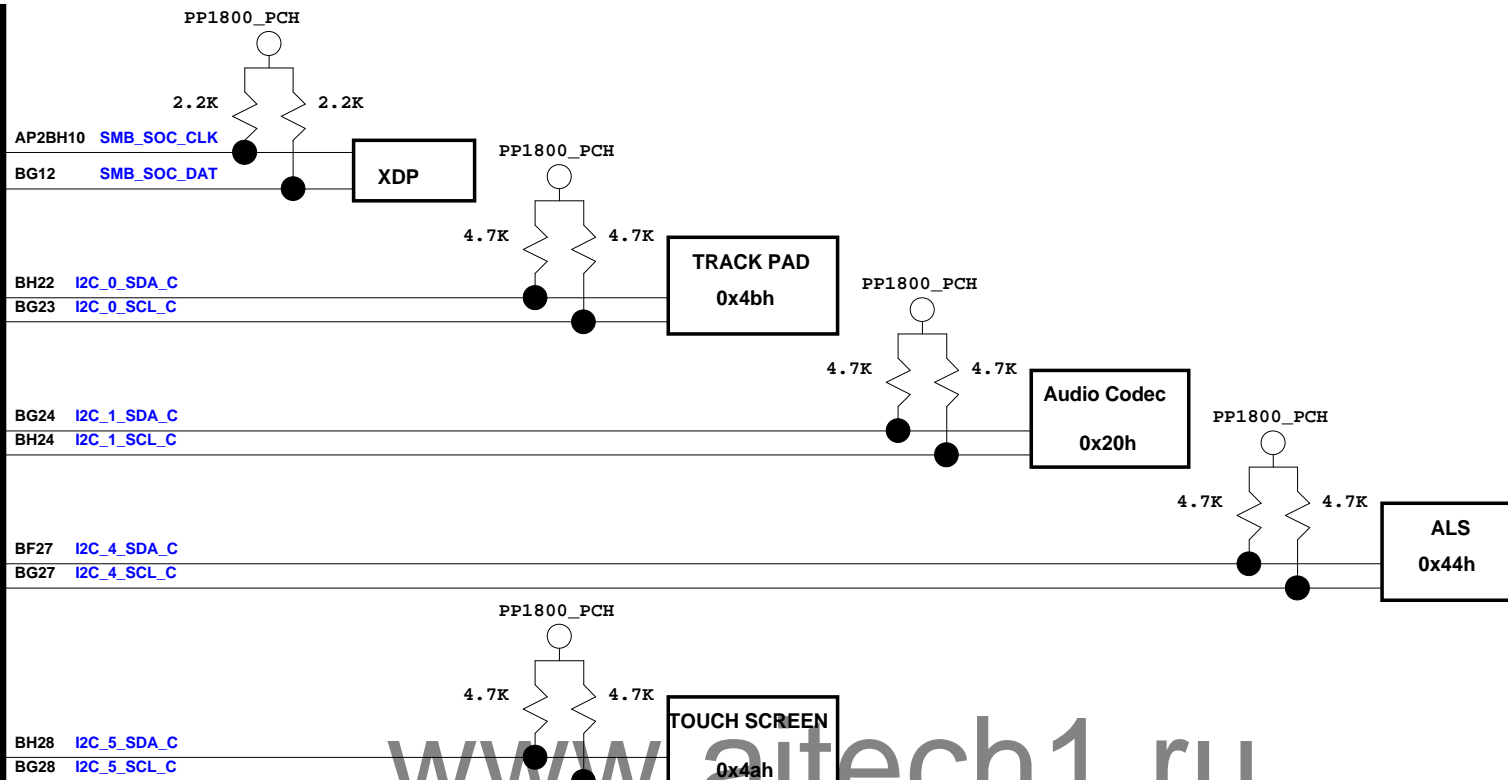
PROJECT :

Size	Document Number	Rev
	Thermal protect	1A
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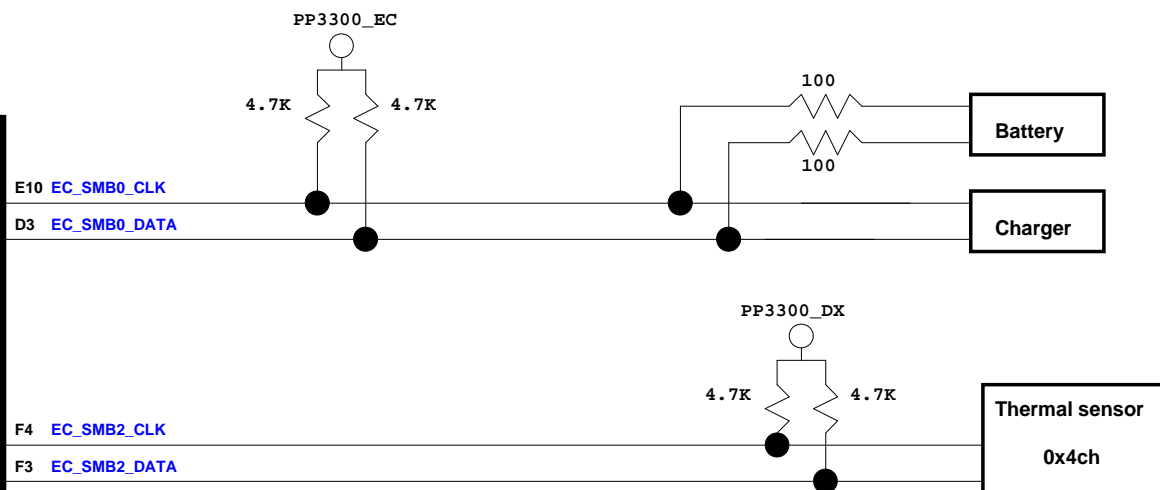


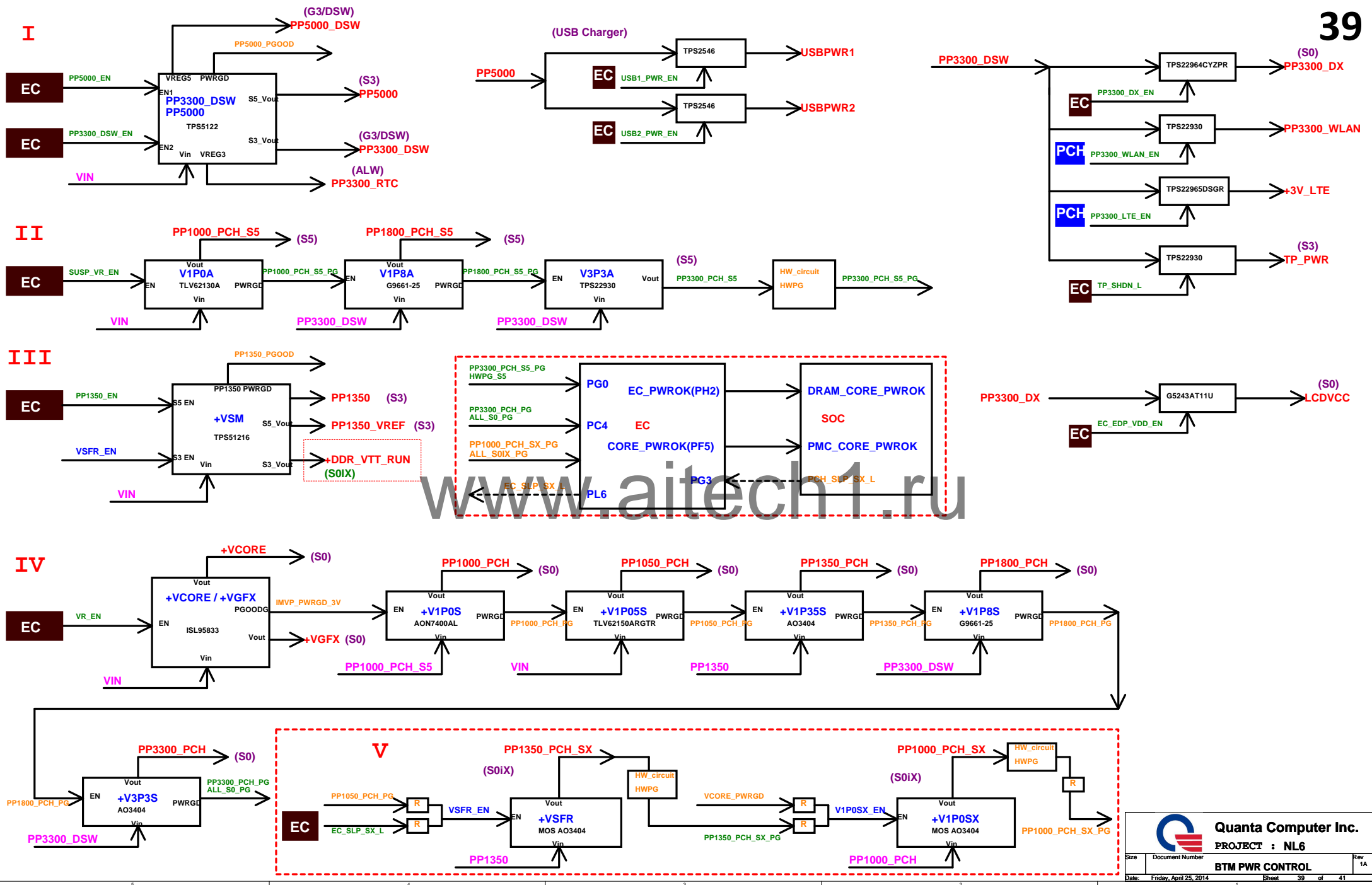
SMBUS
Bay-trail M

I2C



KBC
TI
SMBUS





Model	Version	CHANGE LIST	40
OCX	1A	<p>10-11 101 Change PWR_VCC, C14, R6 (Page 28) 102 Change PWR_VCC, R7 (Page 28) 103 Change PWR1 from 100V_P to 100V_P4 (Page 32) 104 Remove C10, PWR1, MISC_R6 (Page 34) 105 Remove C10, PWR2, MISC_P17 (Page 34) 106 107 Change U11 USB power switch footprint to 0623-5 (Page 17) 108 Unstuffed PWR2 due to PWR10_PWR0 (R6), is 0V tolerance input pin (Page 28) 109 110 Add change R17 from 0P00000007 to 0P00000005 (Page 28) 111 112 Change C126 from *100V-30,8 to *100V-30,8 Due to height limit (Page 24) 113 Change UMR3 3.300 0R on source (Page 24) 114 Change R488 from 5,6 to 5,2, remove R479, R477, merge UMR06_UVR5_012A, UMR06_UVR5_012A, a UMR06_UVR5_012A (Page 9) 115 Change R434 from 5,4 to 5,2, remove R437, merge UMR06_UVR5_012A, a UMR06_UVR5_012A, They are of the same power state and rail (Page 9) 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000 1001 1002 1003 1004 1005 1006 1007 1008 1009 1010 1011 1012 1013 1014 1015 1016 1017 1018 1019 1020 1021 1022 1023 1024 1025 1026 1027 1028 1029 1030 1031 1032 1033 1034 1035 1036 1037 1038 1039 1040 1041 1042 1043 1044 1045 1046 1047 1048 1049 1050 1051 1052 1053 1054 1055 1056 1057 1058 1059 1060 1061 1062 1063 1064 1065 1066 1067 1068 1069 1070 1071 1072 1073 1074 1075 1076 1077 1078 1079 1080 1081 1082 1083 1084 1085 1086 1087 1088 1089 1090 1091 1092 1093 1094 1095 1096 1097 1098 1099 1100 1101 1102 1103 1104 1105 1106 1107 1108 1109 1110 1111 1112 1113 1114 1115 1116 1117 1118 1119 1120 1121 1122 1123 1124 1125 1126 1127 1128 1129 1130 1131 1132 1133 1134 1135 1136 1137 1138 1139 1140 1141 1142 1143 1144 1145 1146 1147 1148 1149 1150 1151 1152 1153 1154 1155 1156 1157 1158 1159 1160 1161 1162 1163 1164 1165 1166 1167 1168 1169 1170 1171 1172 1173 1174 1175 1176 1177 1178 1179 1180 1181 1182 1183 1184 1185 1186 1187 1188 1189 1190 1191 1192 1193 1194 1195 1196 1197 1198 1199 1200 1201 1202 1203 1204 1205 1206 1207 1208 1209 1210 1211 1212 1213 1214 1215 1216 1217 1218 1219 1220 1221 1222 1223 1224 1225 1226 1227 1228 1229 1230 1231 1232 1233 1234 1235 1236 1237 1238 1239 1240 1241 1242 1243 1244 1245 1246 1247 1248 1249 1250 1251 1252 1253 1254 1255 1256 1257 1258 1259 1260 1261 1262 1263 1264 1265 1266 1267 1268 1269 1270 1271 1272 1273 1274 1275 1276 1277 1278 1279 1280 1281 1282 1283 1284 1285 1286 1287 1288 1289 1290 1291 1292 1293 1294 1295 1296 1297 1298 1299 1300 1301 1302 1303 1304 1305 1306 1307 1308 1309 1310 1311 1312 1313 1314 1315 1316 1317 1318 1319 1320 1321 1322 1323 1324 1325 1326 1327 1328 1329 1330 1331 1332 1333 1334 1335 1336 1337 1338 1339 1340 1341 1342 1343 1344 1345 1346 1347 1348 1349 1350 1351 1352 1353 1354 1355 1356 1357 1358 1359 1360 1361 1362 1363 1364 1365 1366 1367 1368 1369 1370 1371 1372 1373 1374 1375 1376 1377 1378 1379 1380 1381 1382 1383 1384 1385 1386 1387 1388 1389 1390 1391 1392 1393 1394 1395 1396 1397 1398 1399 1400 1401 1402 1403 1404 1405 1406 1407 1408 1409 1410 1411 1412 1413 1414 1415 1416 1417 1418 1419 1420 1421 1422 1423 1424 1425 1426 1427 1428 1429 1430 1431 1432 1433 1434 1435 1436 1437 1438 1439 1440 1441 1442 1443 1444 1445 1446 1447 1448 1449 1450 1451 1452 1453 1454 1455 1456 1457 1458 1459 1460 1461 1462 1463 1464 1465 1466 1467 1468 1469 1470 1471 1472 1473 1474 1475 1476 1477 1478 1479 1480 1481 1482 1483 1484 1485 1486 1487 1488 1489 1490 1491 1492 1493 1494 1495 1496 1497 1498 1499 1500 1501 1502 1503 1504 1505 1506 1507 1508 1509 1510 1511 1512 1513 1514 1515 1516 1517 1518 1519 1520 1521 1522 1523 1524 1525 1526 1527 1528 1529 1530 1531 1532 1533 1534 1535 1536 1537 1538 1539 1540 1541 1542 1543 1544 1545 1546 1547 1548 1549 1550 1551 1552 1553 1554 1555 1556 1557 1558 1559 1560 1561 1562 1563 1564 1565 1566 1567 1568 1569 1570 1571 1572 1573 1574 1575 1576 1577 1578 1579 1580 1581 1582 1583 1584 1585 1586 1587 1588 1589 1590 1591 1592 1593 1594 1595 1596 1597 1598 1599 1600 1601 1602 1603 1604 1605 1606 1607 1608 1609 1610 1611 1612 1613 1614 1615 1616 1617 1618 1619 1620 1621 1622 1623 1624 1625 1626 1627 1628 1629 1630 1631 1632 1633 1634 1635 1636 1637 1638 1639 1640 1641 1642 1643 1644 1645 1646 1647 1648 1649 1650 1651 1652 1653 1654 1655 1656 1657 1658 1659 1660 1661 1662 1663 1664 1665 1666 1667 1668 1669 1670 1671 1672 1673 1674 1675 1676 1677 1678 1679 1680 1681 1682 1683 1684 1685 1686 1687 1688 1689 1690 1691 1692 1693 1694 1695 1696 1697 1698 1699 1700 1701 1702 1703 1704 1705 1706 1707 1708 1709 1710 1711 1712 1713 1714 1715 1716 1717 1718 1719 1720 1721 1722 1723 1724 1725 1726 1727 1728 1729 1730 1731 1732 1733 1734 1735 1736 1737 1738 1739 1740 1741 1742 1743 1744 1745 1746 1747 1748 1749 1750 1751 1752 1753 1754 1755 1756 1757 1758 1759 1760 1761 1762 1763 1764 1765 1766 1767 1768 1769 1770 1771 1772 1773 1774 1775 1776 1777 1778 1779 1780 1781 1782 1783 1784 1785 1786 1787 1788 1789 1790 1791 1792 1793 1794 1795 1796 1797 1798 1799 1800 1801 1802 1803 1804 1805 1806 1807 1808 1809 1810 1811 1812 1813 1814 1815 1816 1817 1818 1819 1820 1821 1822 1823 1824 1825 1826 1827 1828 1829 1830 1831 1832 1833 1834 1835 1836 1837 1838 1839 1840 1841 1842 1843 1844 1845 1846 1847 1848 1849 1850 1851 1852 1853 1854 1855 1856 1857 1858 1859 1860 1861 1862 1863 1864 1865 1866 1867 1868 1869 1870 1871 1872 1873 1874 1875 1876 1877 1878 1879 1880 1881 1882 1883 1884 1885 1886 1887 1888 1889 1890 1891 1892 1893 1894 1895 1896 1897 1898 1899 1900 1901 1902 1903 1904 1905 1906 1907 1908 1909 1910 1911 1912 1913 1914 1915 1916 1917 1918 1919 1920 1921 1922 1923 1924 1925 1926 1927 1928 1929 1930 1931 </p>	

CHANGE LIST

Model

Version

NL6

PVT1

2/20

1. un-stuff R156 for SERIRQ skipped (Page14)
2. change power rail of Q35,Q36,Q37,Q44 from PP1800_PCH_S5 to PP1800_PCH for PP1800_PCH leakage issue in S3 mode (Page14)
3. unstuff R337 for S3 leakage issue(Page 11)
4. Delete LED2, R127 (Page 22,27)
5. Change LED1 type to right angle , same as 0C7 (Page22)
6. unstuff R454,Q33,Q144 for auto power on issue when insert battery first time(Page 26)
7. change PR130 to 124K ohm for efficiency improvement (Page 33)
8. change PL7/PL4 to 0.47uH and PR30/PR62 to 0ohm for efficiency improvement (Page 28)
9. unstuff NUT of Hole4,Hole5(Page 25)

PVT2

3/19

1. Disconnect SPI SIO I/F (Page6, 27)
2. Delete SPI_SIO Interface,Q35,Q36,Q37,Q44,R486,R484,R485,R483,R426,R429,R427,R428 (Page14)
3. reserve C377 on SD CLK for EMI (Page 5)
4. reserve R483 for CLKRUN# disable (Page 7)
5. change level shifter of PMC_SUSCLK1,LTE_DISABLE#,LTE_WAKE#,PMC_SUSCLK0,SOC_PMC_WAKE#,WIFI_DISABLE# to double inverter for S3 leakage issue (Page 15)
6. stuff C372 for EMI issue(Page 16)
7. add PD13 for S3 leakage(Page 28)
8. reserve C330 for EMI request (Page 25)
9. reserve placeholder R212,R218 for additional RAM ID (Page 7)
10. change bi-direction level shifter of LTE_DISABLE#,LTE_WAKE#,SOC_PMC_WAKE#,WIFI_DISABLE# to double inverter for S3 leakage issue, and PMC_SUSCLK0 and PMC_SUSCLK1 to buffer type (Page 15)
11. Reserve load switch(U1007,C391,R623) for touch screen power(Page 17)
12. reserve R91 0 ohm on SIM_DET line for difference design of various cards(Page 15)
13. Change below 0 ohm to short pad for cost saving:
0402: R180,R197,R204,R123,R131,R139,R455,R462,R103,R414,R383,R375,R381,R379,R183,R452,R457,R58,R165,R468,R448,R107,R424,R449,R343,R385,R54,R378,R380,R430,R456,R110,R114,R121,R395,R400,R407,R453,R464,R460,R319,R320,R332,R263,R333,R171,R174,R137,R10,R11,R13,R326,R341,R339,R20,R46,R411,R51,R60,R72,R57,R370,R67,R194,R244,R390,R213,R546,R227,R173,R169
0603: R116,R157,R193,R555,R14,R224,R355,R229,R232,R235,R241,R217,L7,R206
0805: R354,R384,R17,R39
14. Change LED1 to Green/Orange
15. Change C78 to 220uF
16. Add C393 2.2uF at Q33 pin2, change R414 to 1Mohm
17. Add D23 for Pp5000

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